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ILC BEAM-BASED FEEDBACK SYSTEMS OVERVIEW

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We report preliminary results of beam tests of the FONT3 Linear Collider intra-train position feedback system prototype at the Accelerator Test Facility at KEK. The feedback system incorporates a novel beam position monitor (BPM) processor with a latency below 5 nanoseconds, and a kicker driver amplifier with similar low latency. The 56 nanosecond-long bunchtrain in the ATF extraction line was used to test the prototype BPM processor. The achieved latency will allow a demonstration of intra-train feedback on timescales relevant even for the CLIC Linear Collider design.

1. INTRODUCTION

A number of fast beam-based feedback systems are required at the International electron-positron Linear Collider (ILC). At the interaction point (IP) a very fast system, operating on nanosecond timescales within each bunchtrain, is required to compensate for residual vibration-induced jitter on the final-focus magnets by steering the electron and positron beams into collision. A pulse-to-pulse feedback system is envisaged for optimising the luminosity on timescales corresponding to 5 Hz. Slower feedbacks, operating in the 0.1 – 1 Hz range, will control the beam orbit through the Linacs and Beam Delivery System.

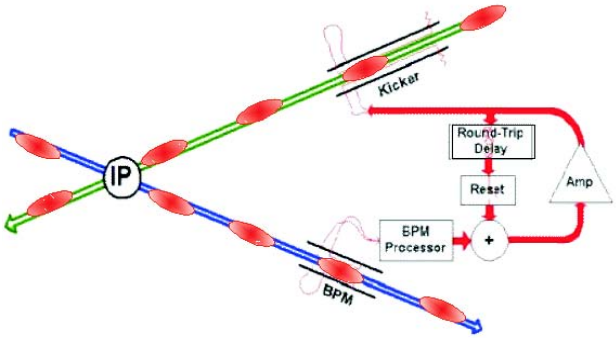

Figure 1: Schematic of IP intra-train feedback system for an interaction region with a crossing angle. The deflection of the outgoing beam is registered in a BPM and a correcting kick applied to the incoming other beam.

The key components of each such system are beam position monitors (BPMs) for registering the beam orbit; fast signal processors to translate the raw BPM pickoff signals into a normalised position output; feedback circuits, including delay loops, for applying gain and taking account of system latency; amplifiers to provide the required output drive signals; and kickers for applying the position (or angle) correction to the beam. A schematic of the IP intra-train feedback is shown in Figure 1, for the case in which the electron and positron beams cross with a small angle.

2. FONT 3

Feedback On Nanosecond Timescales (FONT) is a collaboration between UK academic groups (QMUL, Oxford, Daresbury) and the ILC Group at SLAC with the purpose of prototyping and testing IP feedback components. Two

rounds of earlier tests have taken place (FONT1, FONT2) with the 65 MeV electron beam at the NLC Test Accelerator (NLCTA) at SLAC [1,2]. At NLCTA the train length was c. 170ns, and an ILC-like intra-train feedback system was demonstrated with a latency of 54ns and a correction ratio of 14/1.

Here we report on beam tests of the latest prototype, FONT3, which we operate at the Accelerator Test Facility extraction line at KEK. The current bunchtrain comprises up to 20 electron bunches separated by 2.8ns with a beam energy of c. 1.3 GeV. The total train length of 56ns presents a severe challenge for an intra-train feedback system. Hence we have designed FONT3 as a fast-analogue system with a design goal of 20ns total latency, which includes the beam time-of-flight and signal propagation delays.

A schematic of the experimental configuration in the ATF beamline is illustrated in Figure 2. The layout is functionally equivalent to the ILC intra-train feedback system. An upstream dipole corrector magnet can be used to steer the beam so as to introduce a controllable vertical position offset in stripline BPM ML11X. A signal processor and a feedback circuit provide a correction signal to drive the adjustable-gap stripline kicker [3] so as to steer the beam back into nominal vertical position. BPMs ML12X and ML13X serve as independent witnesses of the beam position. The experimental setup in the extraction line is illustrated in Figure 3.

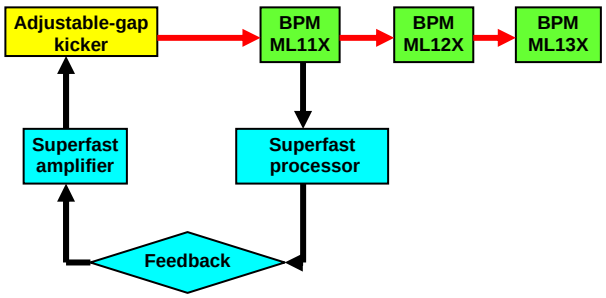

Figure 2: Schematic of the ATF beamline showing location of the kicker, BPMs and feedback system.

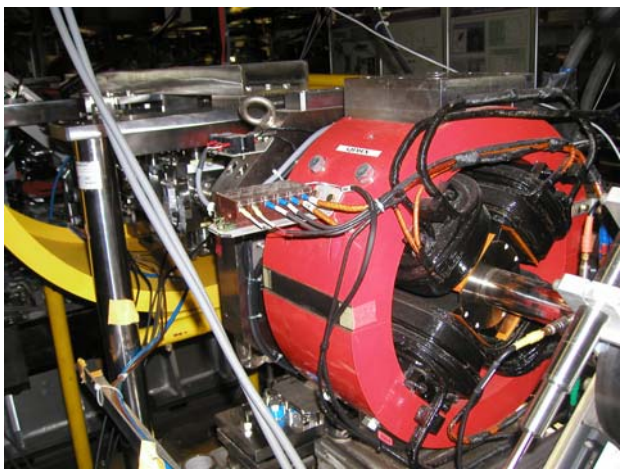

Figure 3: ATF beamline showing the kicker (left) and BPM (right).

The hardware layout is shown in Figures 3 and 4.

The BPM signals were mixed from X-band to baseband in a two-stage down-mixing process with an intermediate frequency stage of 400 MHz. Normalisation by the beam charge was performed in real-time by taking the difference between the top and bottom pickoff signals using logarithmic amplifiers. The correction signal was fed to solid state amplifiers (maximum power roughly 800 W each) which drove the two kickers.

3. SIGNAL PROCESSOR

The design of the BPM signal processor is illustrated in Figure 4. The top and bottom stripline signals are subtracted using a hybrid. The resulting difference signal is band-pass filtered and down-mixed with a 714 MHz local oscillator signal which is phase-locked to the beam. The resulting baseband signal is low-pass filtered. The hybrid, filters and mixer were selected to have latencies of order 1ns, in an attempt to yield a total processor latency of less than 5ns.

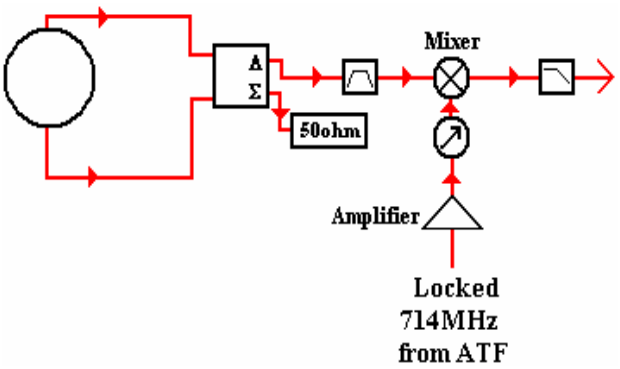

Figure 4: Schematic of BPM signal processor.

The output of the signal processor is illustrated for passage of a single bunch through the BPM in Figure 5. A latency measurement is illustrated in Figure 6, which compares the direct stripline impulse signal with the processor output. The latency is c. 4.3ns.

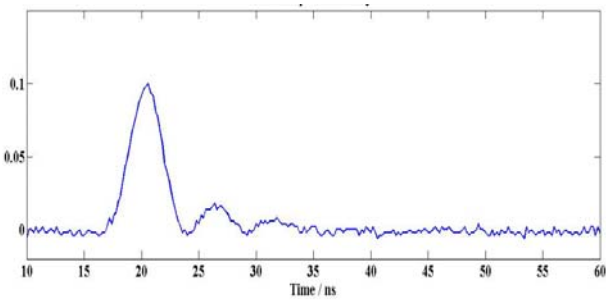

Figure 5: Response of the BPM processor (Volts) to a single electron bunch.

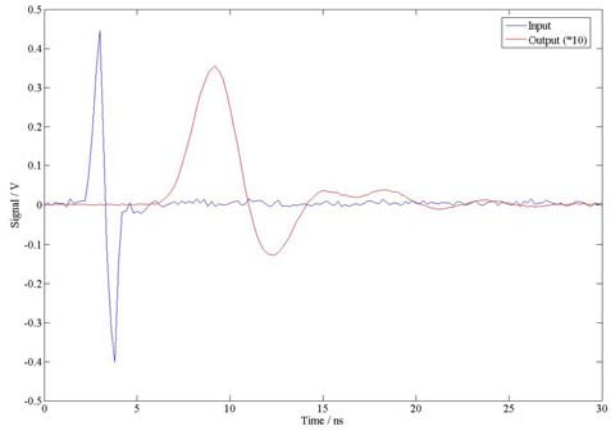

Figure 6: BPM impulse signal (blue) and processor output (red); the time delay represents the latency of the processor.

The position response of the BPM processor is illustrated in Figure 7. The device is linear for beam positions within c. +- 250 microns of the electrical centre. The position resolution was determined using the triplet of BPMs: the predicted position in one BPM was derived by extrapolation from the remaining pair and compared with the measured position on a pulse-by-pulse basis; pulse to pulse position jitter cancels in this method. The difference between measured and predicted positions (Figure 8) provides a measure of the resolution; this was found to be in the range 3-5 microns depending on the BPM.

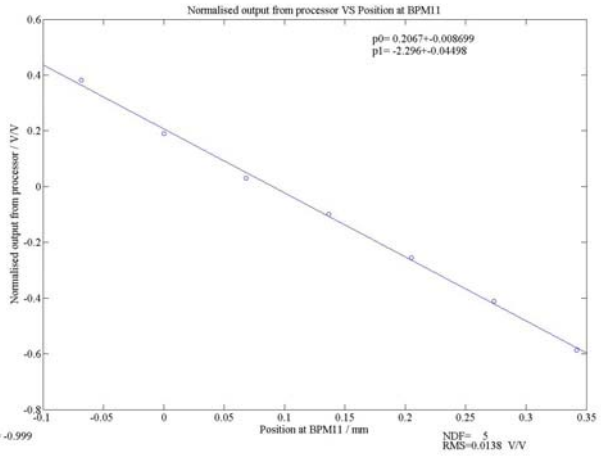

Figure 7: Response of the BPM processor (arbitrary units) to beam position (mm).

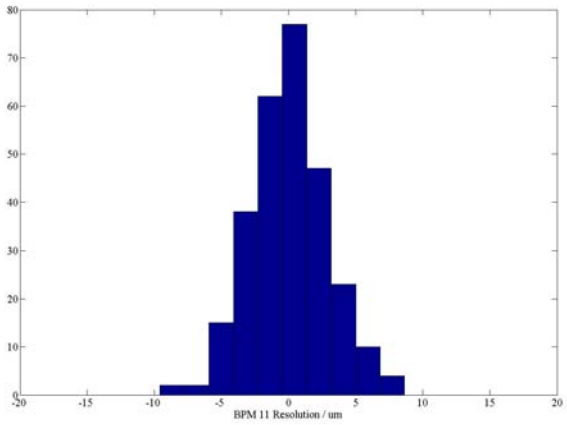

Figure 8: Distribution of measured – predicted position in BPM ML11X (microns) for 40 consecutive beam pulses.

4. BEAM FEEDBACK TESTS

A 100W-level solid-state amplifier, and fast-analogue feedback circuit using the BPM processor output as its input, are being fabricated in preparation for closed-loop feedback tests in the ATF beamline commencing in late May 2005. The amplifier latency has been designed to match that of the BPM processor, yielding c. 10ns total electronics latency. The beam flight time between the kicker and the BPM is c. 4ns, and the return signal path propagation time is c. 5ns. With such a total latency of c. 20ns it should be possible to demonstrate closed-loop feedback, with delay-loop action, within the bunchtrain length of 56ns. The aim is to stabilise the average train position to the level of the BPM resolution of several microns. The amplifier power and BPM resolution are the same as those required for the IP feedback system at the ILC.

5. PLANS FOR FONT4

The ultra-low latency of the FONT3 system was designed to match the bunch spacing (c. 1.ns) and train length (100-300ns) of the 'warm Cu' Linear Collider designs (NLC, GLC, CLIC). In August 2004 superconducting Nb linac technology was selected for the ILC. In this design the bunch spacing is 337ns and the total train length is c. 1ms. Although the FONT3 analogue technology could be deployed at ILC, the longer bunch interval and large number of bunches allow for a digital approach to signal processing, and hence the implementation of more sophisticated feedback algorithms. We are now pursuing the design of such a digital feedback system for ILC. The first prototype, FONT4, will comprise:

- A front-end BPM processor similar to that for FONT3 described here.
- A fast analogue-to-digital converter to digitise the baseband processor output.
- A field programmable gate array (FPGA) device for algorithm deployment.
- A fast digital-to-analogue converter to drive the kicker amplifier.
- A kicker amplifier comprising a modified version of the FONT2 amplifier [2].

The system design is in progress and first tests in the ATF beamline are planned for Spring 2006. The latency target is c. 100ns. This is designed to match both the ILC requirement and the planned initial beam structure at ATF of 3 bunches extracted from the damping ring with a time separation of c. 150ns. This will allow a limited test involving measurement of the first bunch, correction of the second, and delay-loop correction of the third. Eventually it may be possible to extract a longer train of at least 20 bunches with nominal ILC spacing, which would allow more extended feedback algorithm development.

Acknowledgements

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References

[1] FONT1: P.N. Burrows et al, Proceedings PAC, Portland, Oregon, May 2003, p. 687.

[2] FONT2: P.N. Burrows et al, Proceedings EPAC, Lucerne, July 2004, p. 785.

[3] FEATHER: http://acfahep.kek.jp/subg/ir/feather/index.html