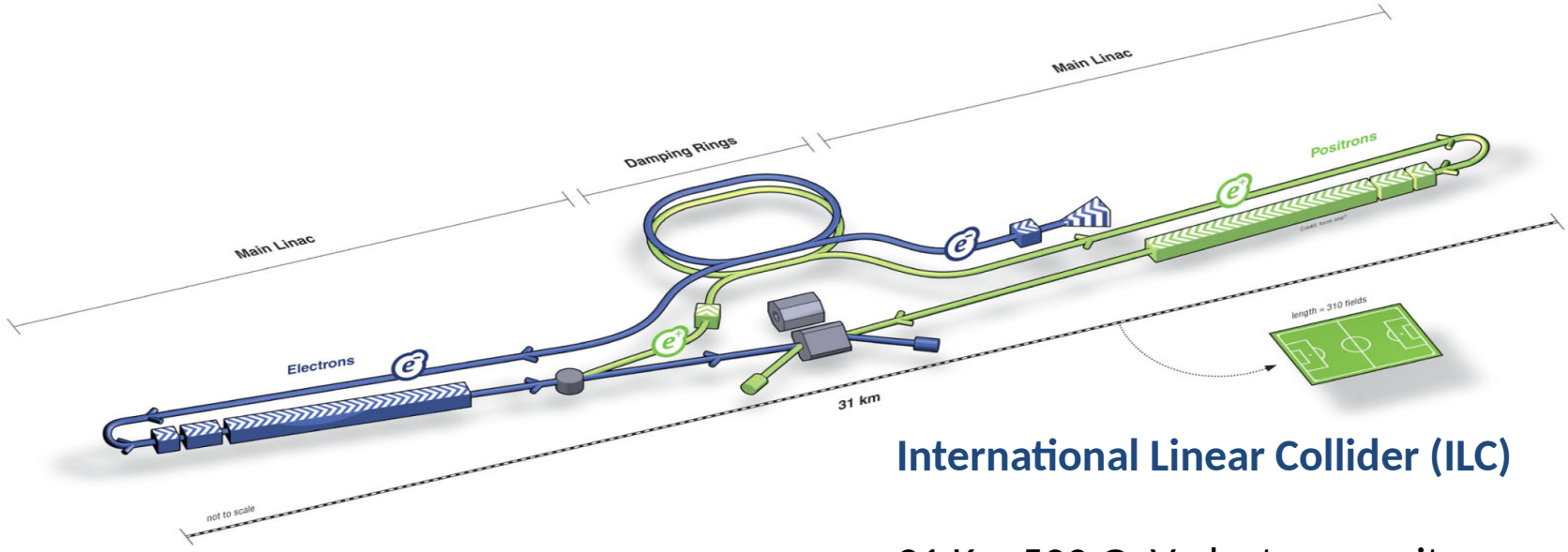
A Fast, Custom FPGA-based Signal Processor and its Applications to Intra-train Beam Stabilisation

Glenn Brian Christian
John Adams Institute for Accelerator Science, University of Oxford
on behalf of Feedback On Nanosecond Timescales (FONT) group

Personal Computers and Particle Accelerator Controls,
Campinas, Brazil, 28 October 2016

Motivation: Luminosity challenge at future linear e+e- collider



International Linear Collider (ILC)

31 Km 500 GeV electron-positron collider / Higgs factory

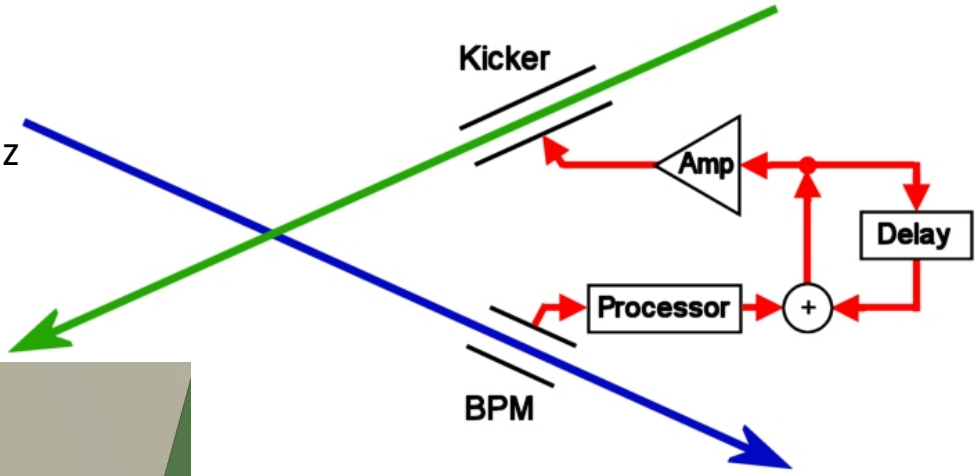
Luminosity goal: 2×10^{34} $cm^{-2}s^{-1}$ requires vertical spot size of 5 nm at Interaction Point

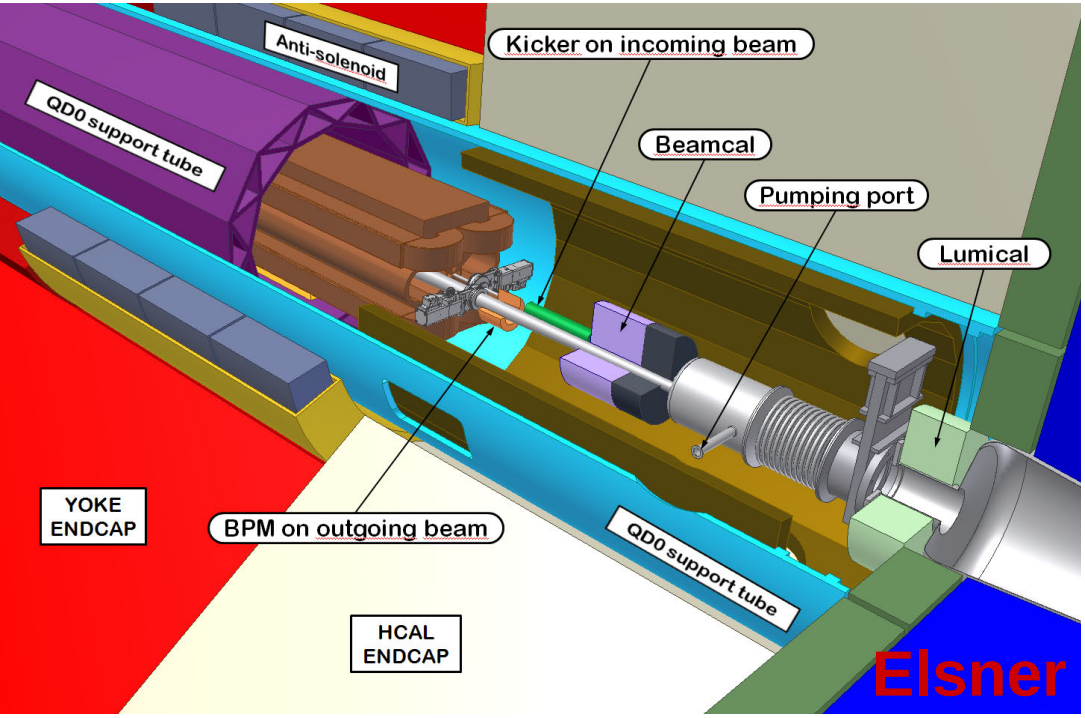
…and even lower for CLIC!

Interaction Point Feedback (IPFB) System for ILC/CLIC

Pulse-to-pulse feedback(s) operating at 5Hz can correct slow variations in beam trajectory (orbit)

- Several local systems cascaded together
- Can not correct frequencies above a few Hz
- Not effective at correcting fast ground motion and facilities noise

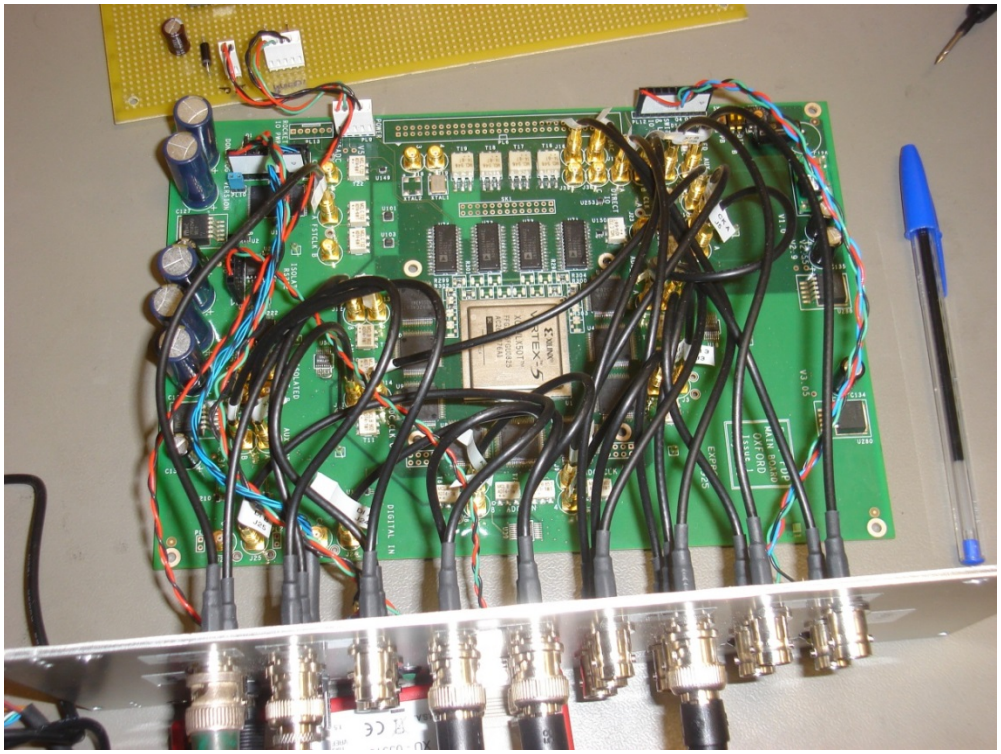


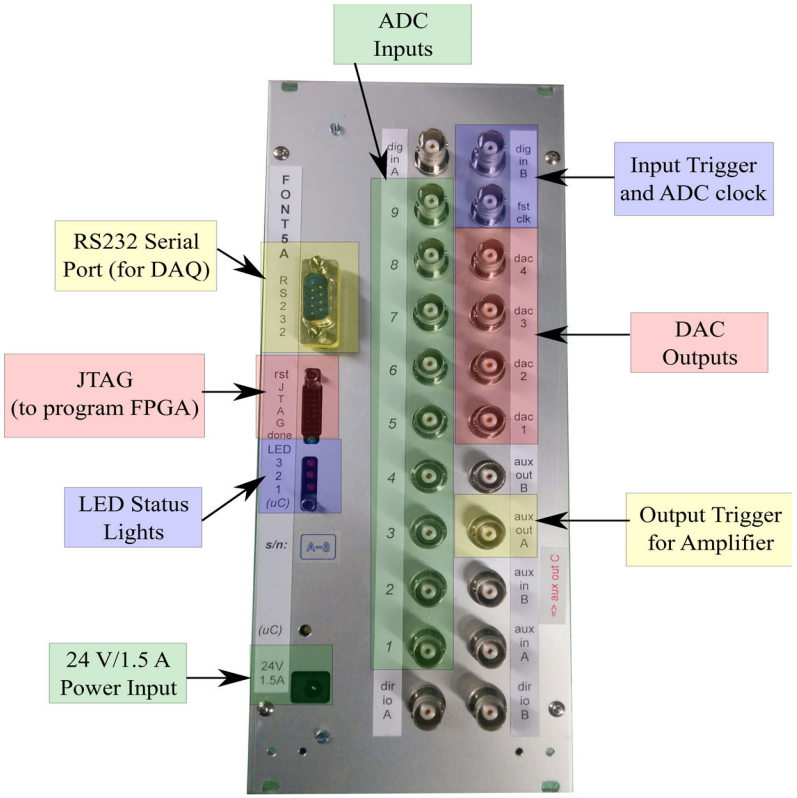


Interaction point Feedback can correct inter-train and intra-train:

- Works by virtue of strong beam-beam deflection at IP
- Large lever arm between IP and BPM ~micron level resolution required
- Low latency system – works on intra-train/bunch-to-bunch timescales

FONT5 Digital Signal Processing board





7 Boards manufactured

- 2 prototype (2008/2010)
- 5 new build (2014/15)
- Parts for 5 more

Based around Xilinx Virtex-5 FPGA (XC5VLXT50)

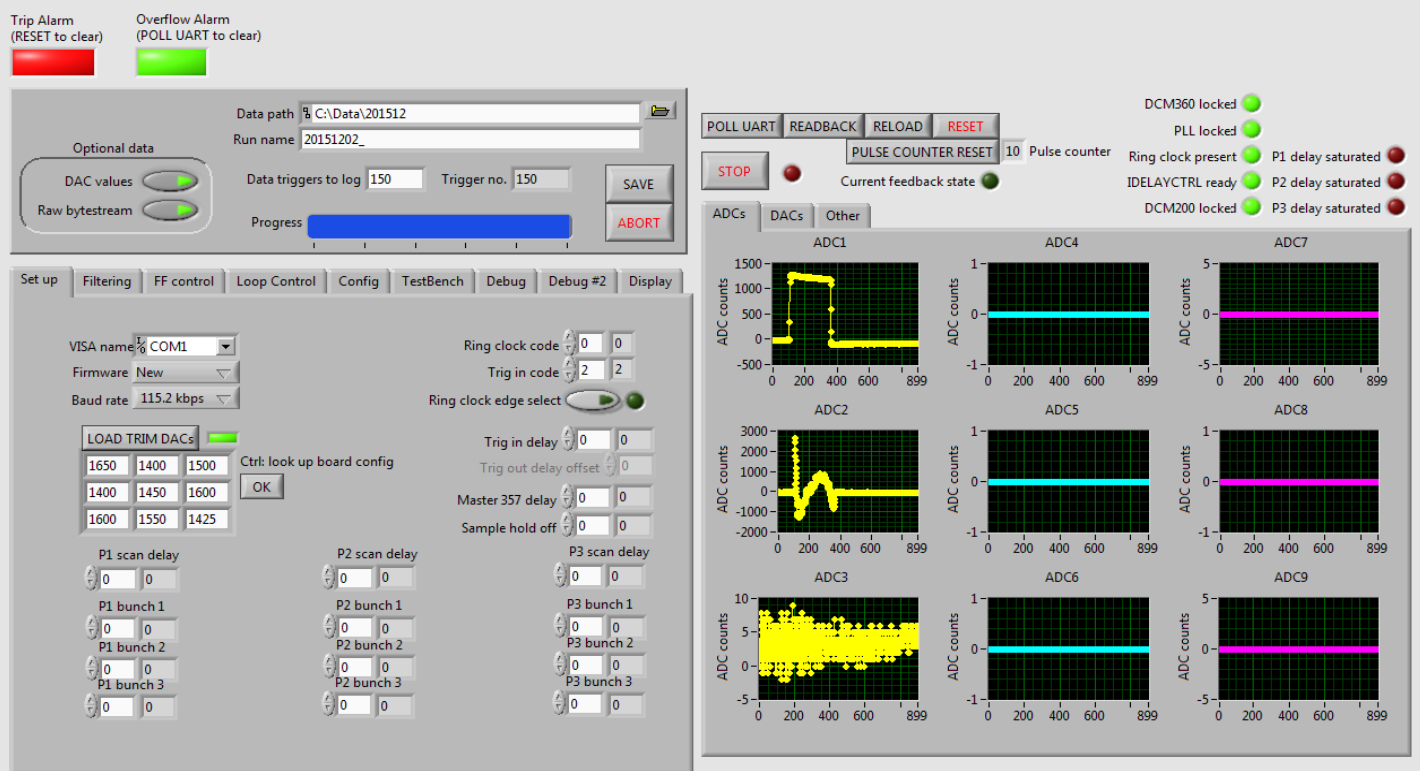
- Max speed 550 MHz
- 2160 Kbit integrated block memory

- **9 ADC channels (3 groups of 3)**
  - TI ADS5474
  - 14 bits (only upper 13 connected)
  - Max sampling speed 400 MHz
  - 3.5 clock cycles latency
  - One common clock per ADC group

- **4 DAC channels**
  - Analog Devices AD9744
  - 14 bit (upper 13 connected)
  - Max conversion speed: 210 MHz
  - ~0.5 cycle latency

- **Fast comparator for external system clock and on-board 40 MHz oscillator for ancillary functions**

Data Acquisition and Control



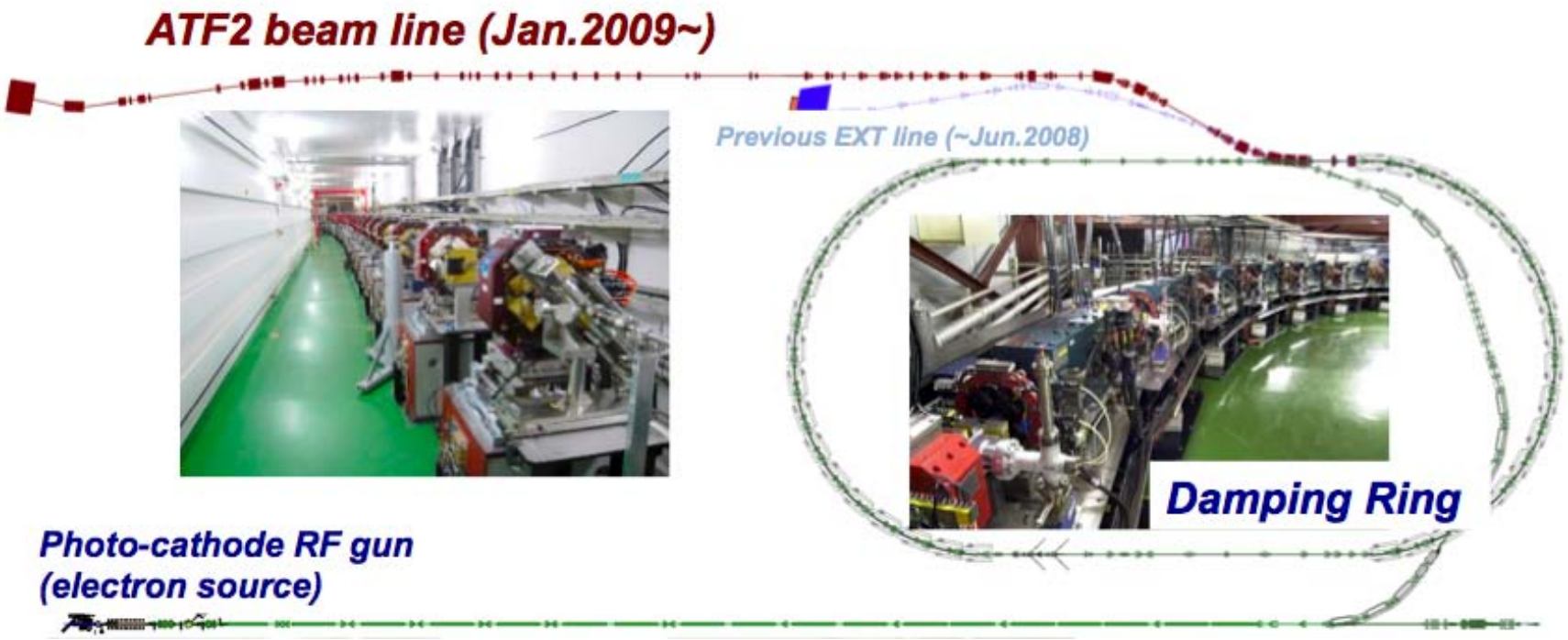
- UART for serial data TX/RX over RS-232
  - Up to 460.8 kbps
  - New build also has USB interface (support data rate ~10 Mbps)
- Up to 128 7-bit control registers in the firmware for:
  - Switch controls
  - Variables
  - RAM addressing
  - Commands

LabVIEW DAQ software

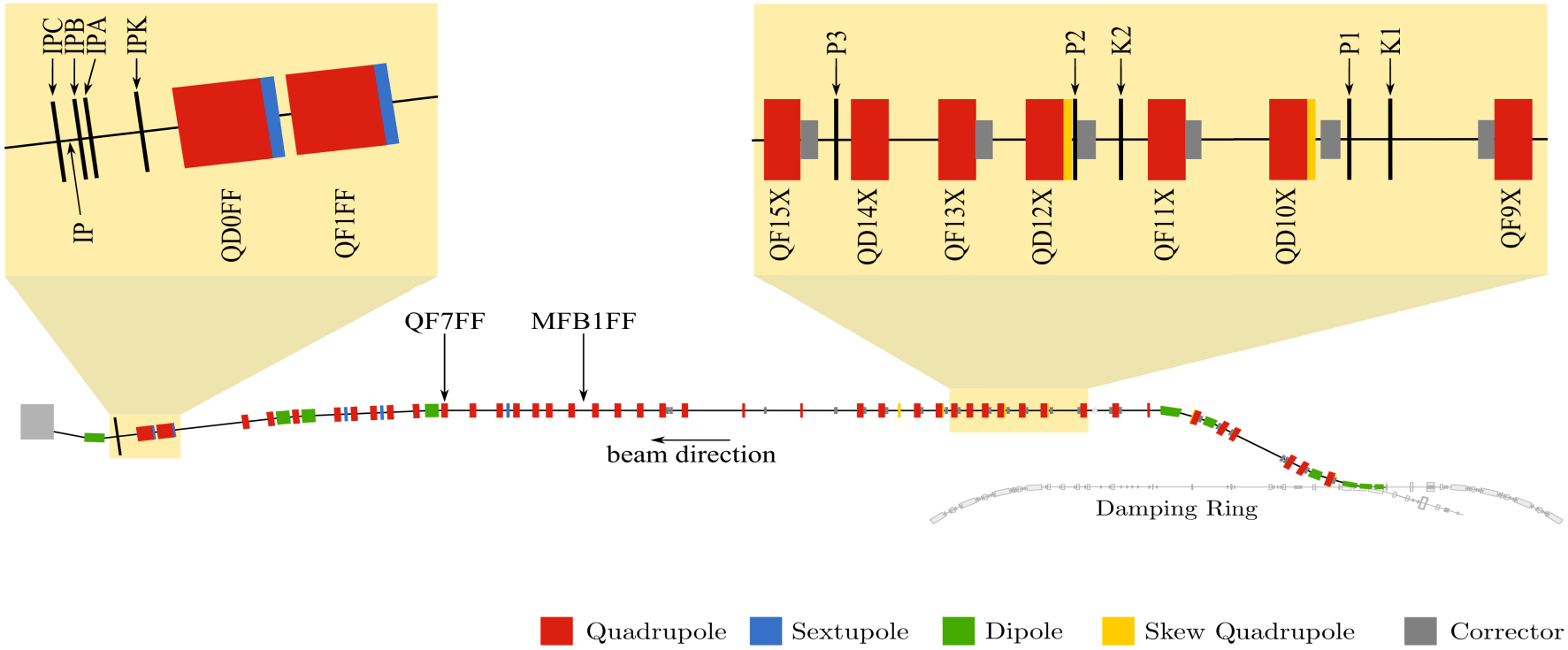
- Display and record data
- Send commands/variables/load RAMs
- Publish data, CR readbacks, and status bytes to EPICS, and read in data from EPICS, via NI EPICS Server/Client
- Automate system set-up: scans, calibrations etc

ATF2 project at KEK

- ATF2 - Scaled-down mock-up of the ILC final focus optics in ATF extraction line
- Goals:
  1) 37 nm vertical spot size at focal point (IP)
     - Small spot-size (~40 nm) reproducibly achieved, but for low-bunch charge
  2) Demonstrate nanometre-level stability at IP
     - Requires bunch-to-bunch feedback and high resolution cavity BPMs in IP region
- Can extract up to three bunches from Damping Ring with ILC-like time structure (~150 ns bunch spacing)

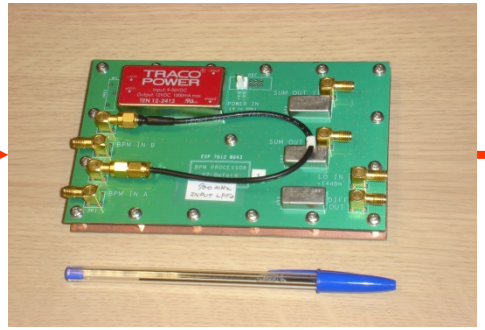


FONT5 upstream feedback system



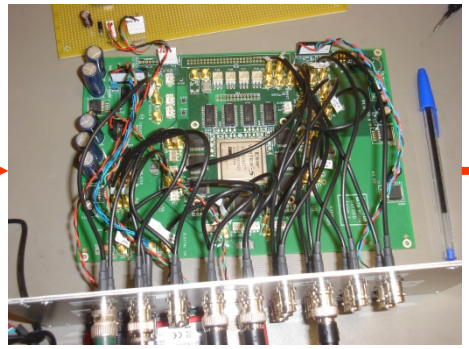
- Two phase FB (position and angle) system to stabilise beam to the 1 micron level at entrance to FF
- Bunch-by-bunch system (measure first bunch, correct subsequent bunches in train)
- 3 stripline BPMs (on movers), 2 stripline kickers

FONT5 Hardware

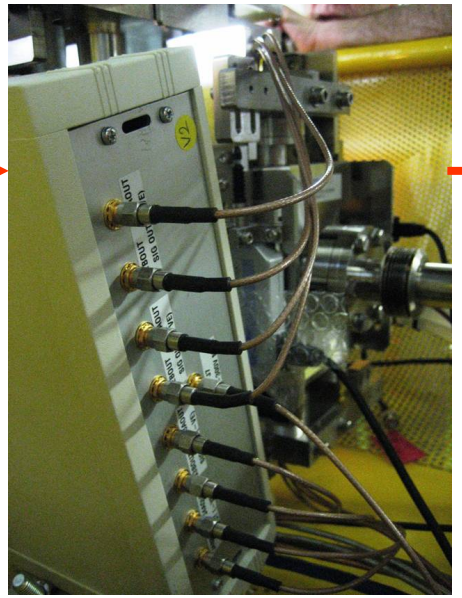


Analogue Front-end

BPM processor

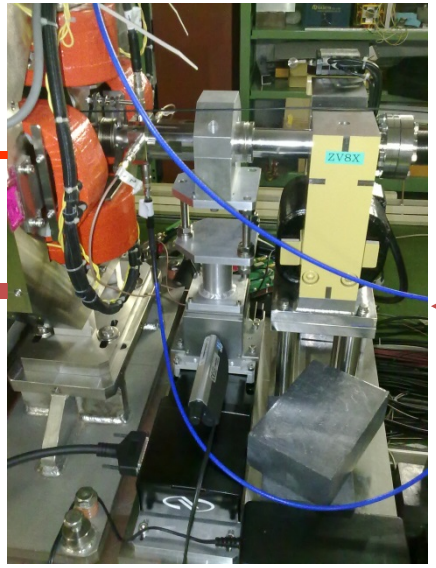


FPGA-based digital processor



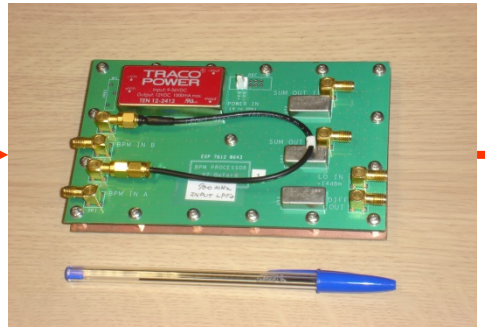
Kicker drive amplifier

Strip-line kicker



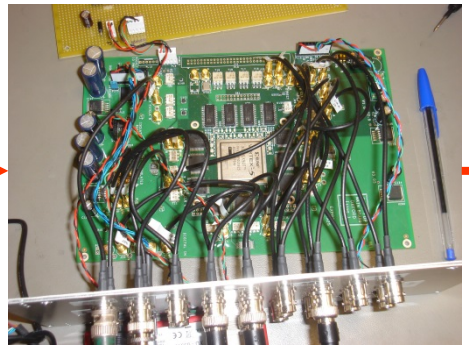
Strip-line BPM with mover system

FONT5 Hardware

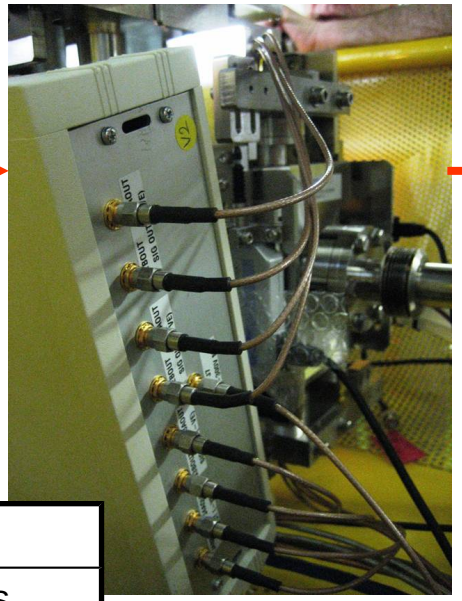


Analogue Front-end

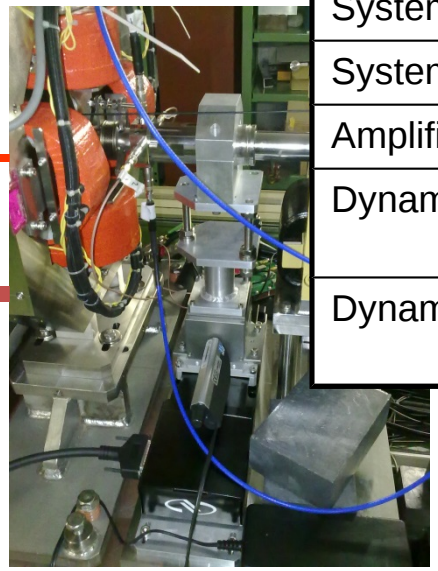
BPM processor



FPGA-based digital processor



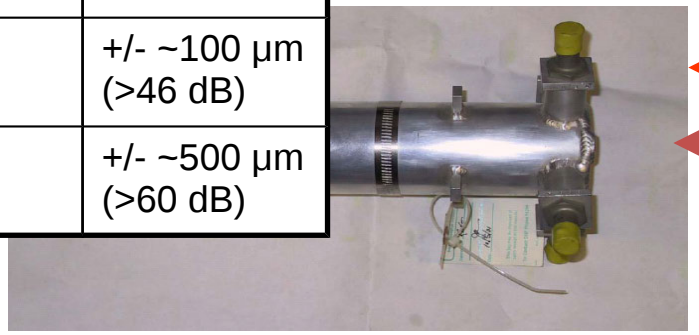
cker drive amplifier



Strip-line BPM with mover system

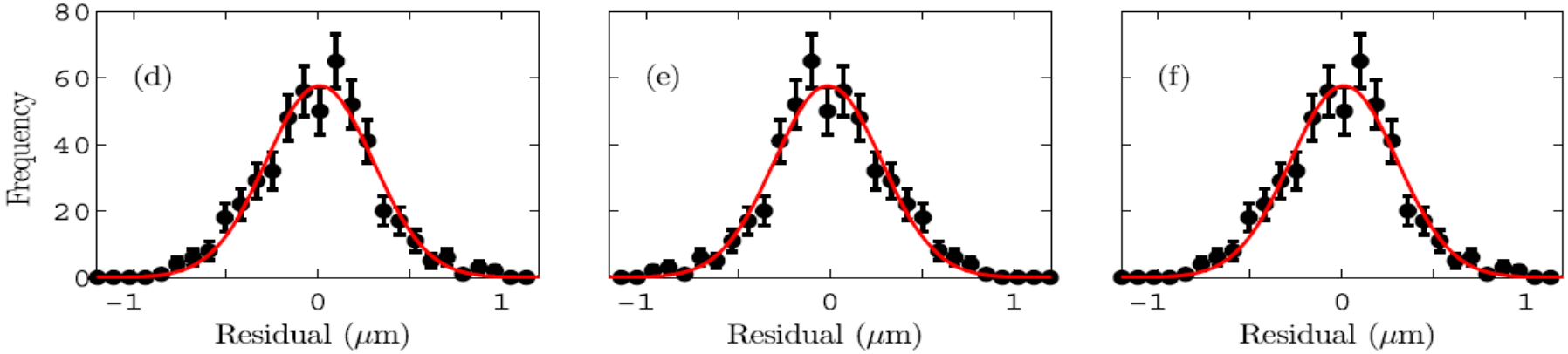
System Resolution (BPM processor)	<1 μm
System Latency	<150 ns
Amplifier/ Kicker Bandwidth	~30 MHz
Dynamic Range of feedback system	+/- ~100 μm (>46 dB)
Dynamic range of the BPM system	+/- ~500 μm (>60 dB)

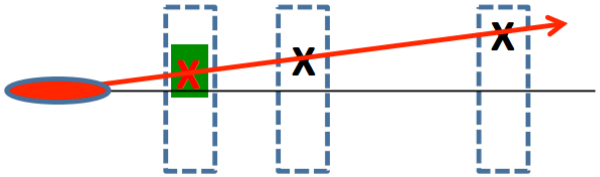
System parameters



Strip-line kicker

Stripline BPM resolution





σ = 291 +/- 10 nm at 1 nC bunch charge

Linear range +/- 500 microns

PHYSICAL REVIEW SPECIAL TOPICS - ACCELERATORS AND BEAMS **18,** 032803 (2015)

Design and performance of a high resolution, low latency stripline beam position monitor system

R. J. Apsimon,* D. R. Bett,† N. Blaskovic Kraljevic, P. N. Burrows, G. B. Christian,‡ C. I. Clarke,§ B. D. Constance, H. Dabiri Khah, M. R. Davis, C. Perry, J. Resta López,‖ and C. J. Swinson¶

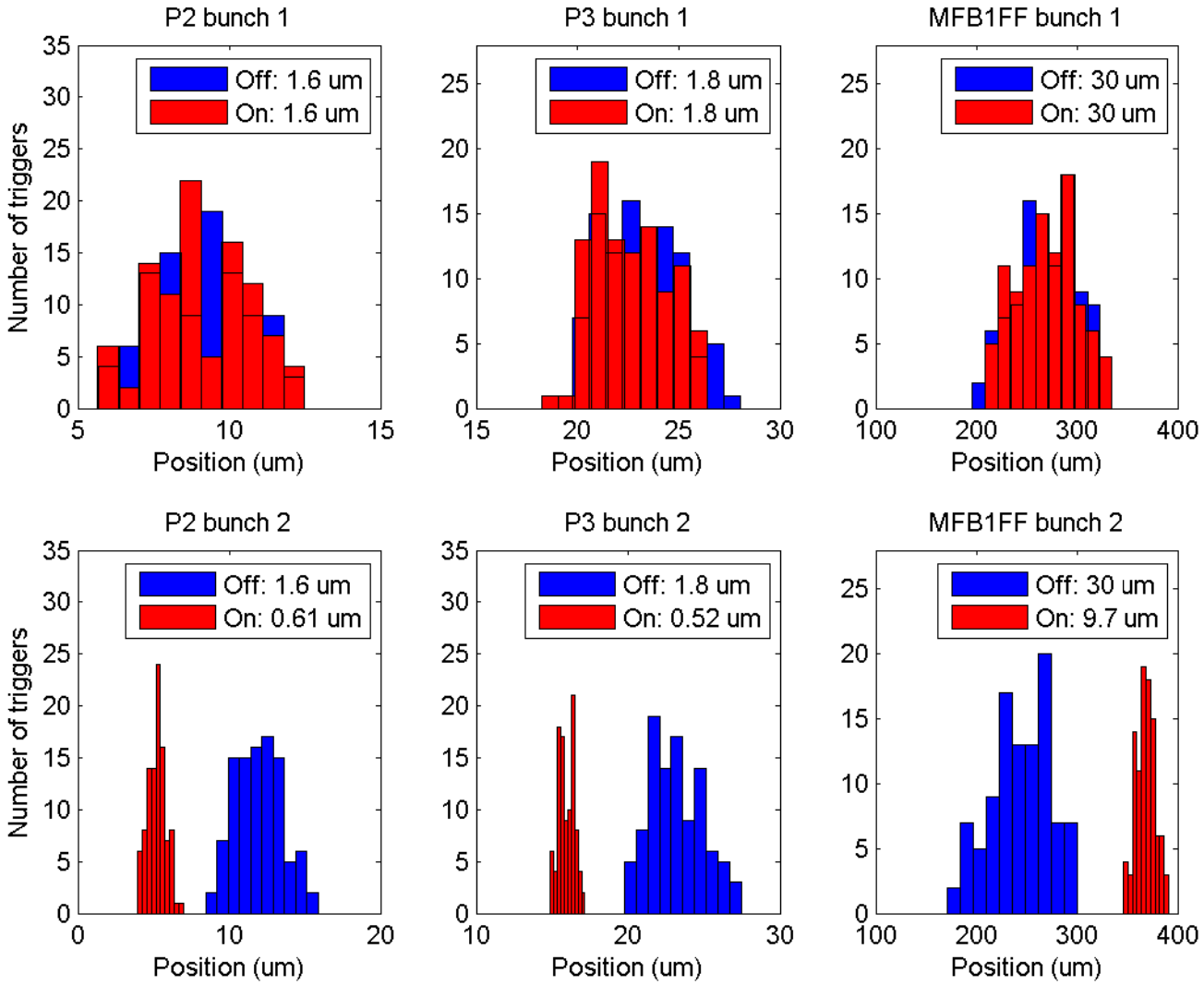
John Adams Institute for Accelerator Science at University of Oxford, Denys Wilkinson Building, Keble Road, Oxford OX1 3RH, United Kingdom

(Received 1 October 2014; published 19 March 2015)

A high-resolution, low-latency beam position monitor (BPM) system has been developed for use in particle accelerators and beam lines that operate with trains of particle bunches with bunch separations as low as several tens of nanoseconds, such as future linear electron-positron colliders and free-electron lasers. The system was tested with electron beams in the extraction line of the Accelerator Test Facility at the High Energy Accelerator Research Organization (KEK) in Japan. It consists of three stripline BPMs instrumented with analogue signal-processing electronics and a custom digitizer for logging the data. The design of the analogue processor units is presented in detail, along with measurements of the system performance. The processor latency is 15.6 ± 0.1 ns. A single-pass beam position resolution of 291 ± 10 nm has been achieved, using a beam with a bunch charge of approximately 1 nC.

Published PRST-AB, March 2015:
http://dx.doi.org/10.1103/PhysRevSTAB.18.032803

FONT5 Upstream Feedback Results 2-bunch (182 ns spacing)

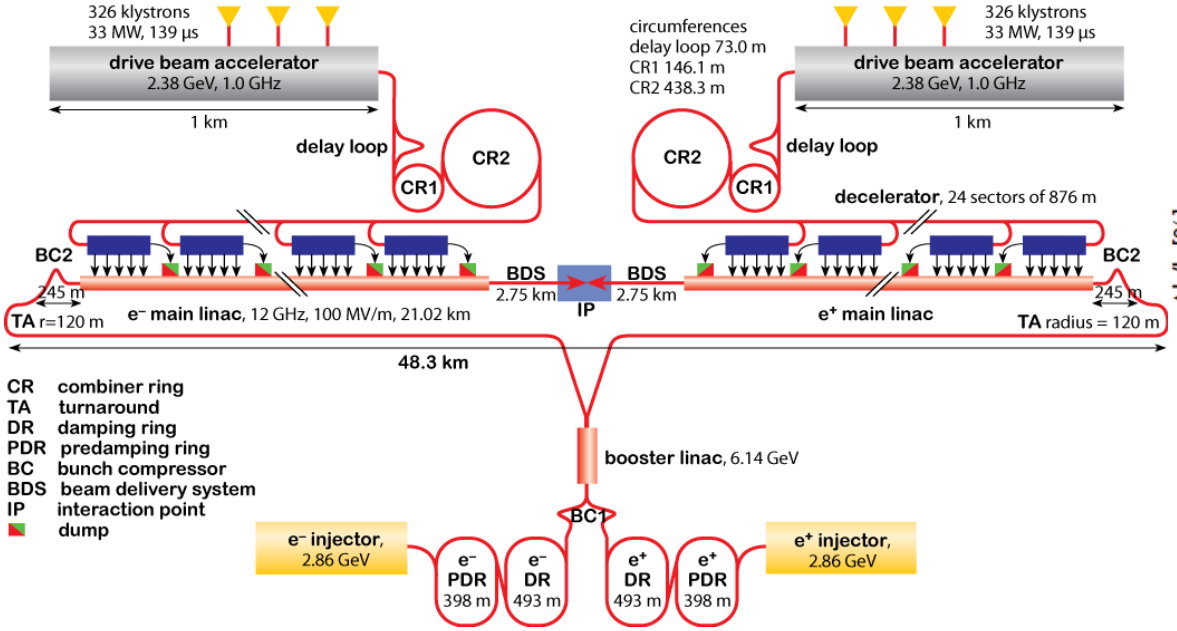


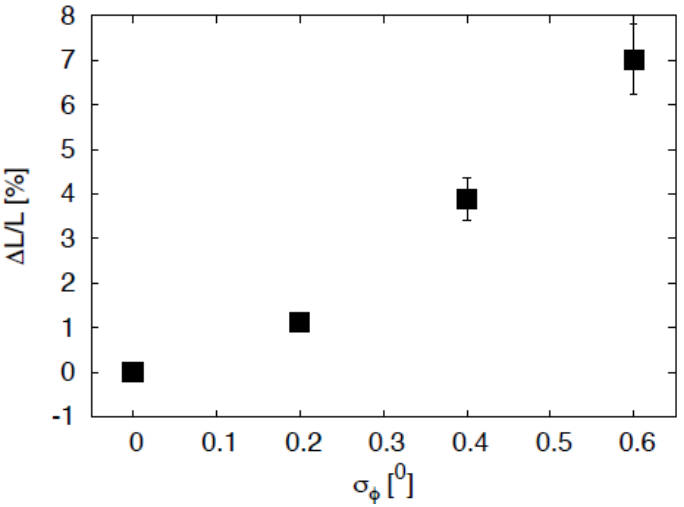
Factor ~3 correction 'in-loop' is preserved at witness BPM, MFB1FF, 30 m downstream

FONT5 upstream system meets ILC requirements, in terms of:

- Measurement sensitivity
- Correction range (energy scaled)
- Latency

CLIC drive beam phase Feed-forward

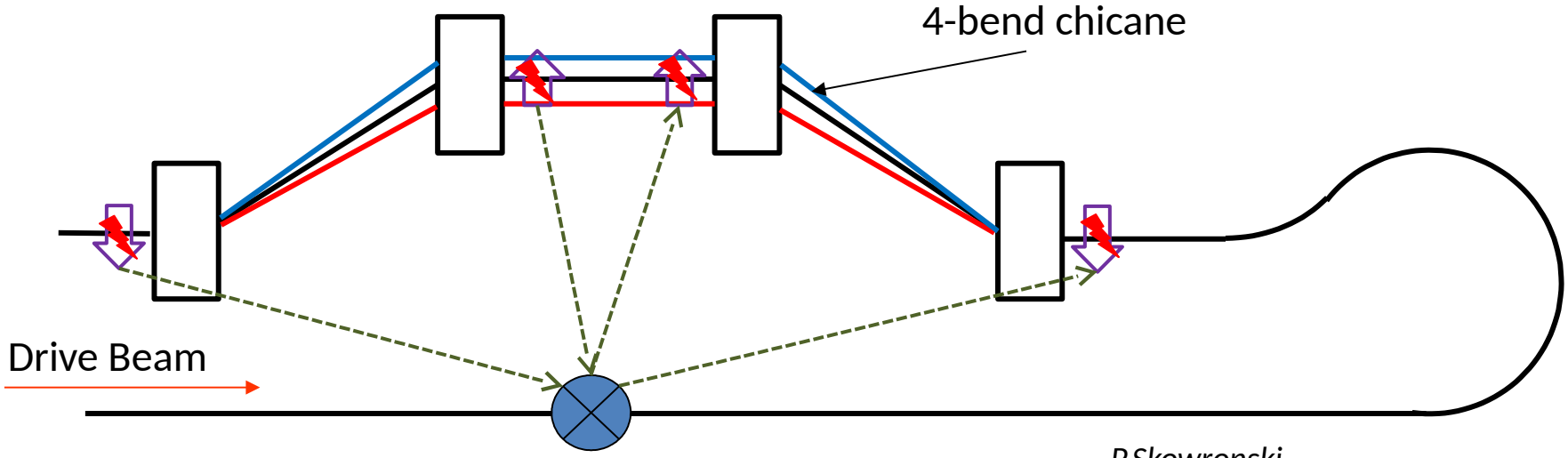




- Problem: For efficient transfer of energy, phase of the decelerated drive beam should precisely match the arrival of the main beam at the cavities.
  - 1 % luminosity loss caused by 0.2 degree phase error, due to energy jitter.
  - Goal: implement system to detect and correct phase error down to less than 0.2° at 12 GHz (< 50 fs).
  - Collaboration between CERN, JAI, and INFN Frascati

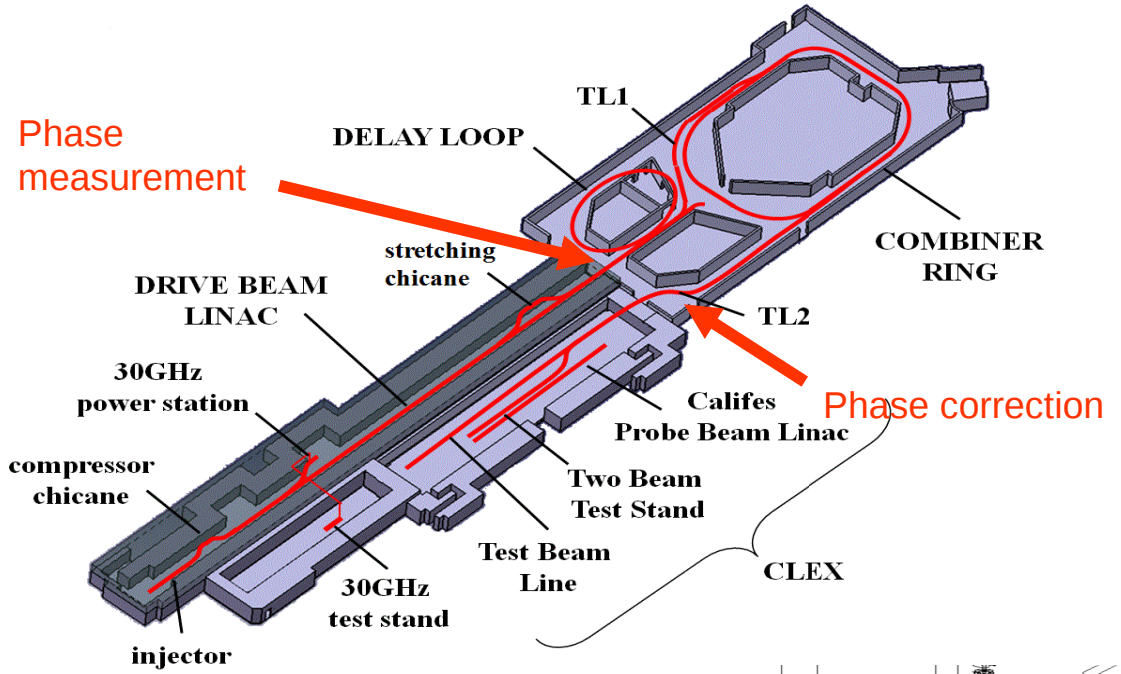
CLIC drive beam phase feedforward

- Instrument each turnaround with feed-forward system:
  - Measure phase at TA entrance and correct with 4-bend magnetic chicane – compensate phase error, changing TOF in chicane.
    - 10 degree correction range, +/- 375 µrad at each bend – 4 kickers per bend
  - ‘Phase monitors’ (INFN Frascati) + readout electronics (CERN)
    - ~20 fs resolution, 100 MHz bandwidth
  - Amplifiers (JAI Oxford)
    - ~500 kW peak power per kicker, ~ 70 MHz bandwidth
  - Kickers (INFN Frascati)
    - 1 metre active length striplines – 16 per turnaround
- System replicated at each of 48 turnarounds at CLIC!



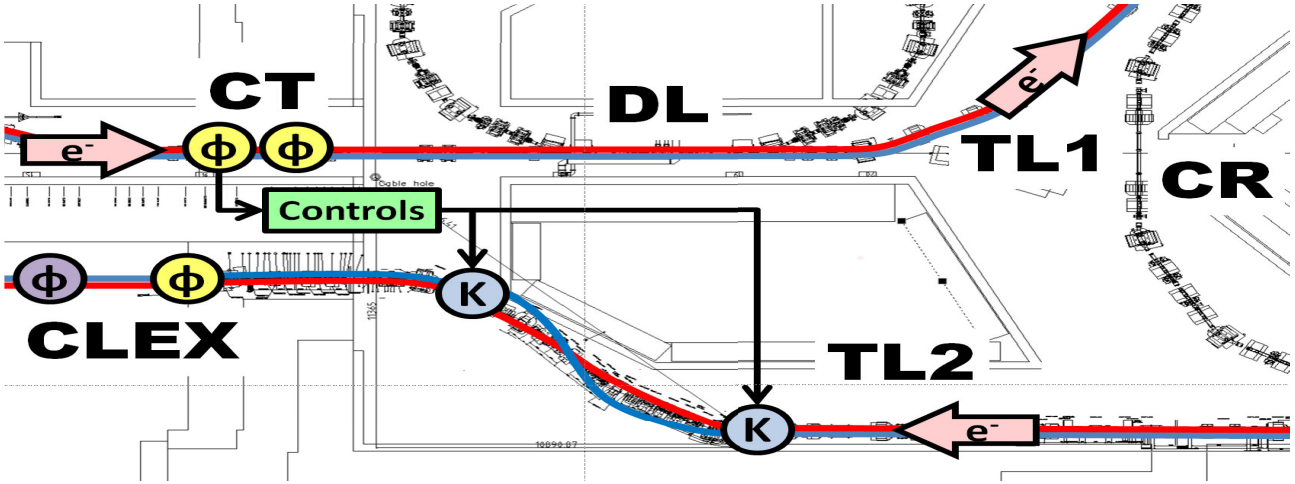
P.Skowronski

CLIC Phase Feedforward Demonstration at CTF3



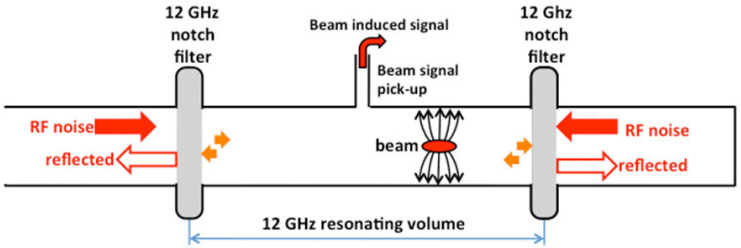
Measure the phase offset upstream, TL1, and correct with 2-kicker system in TL2

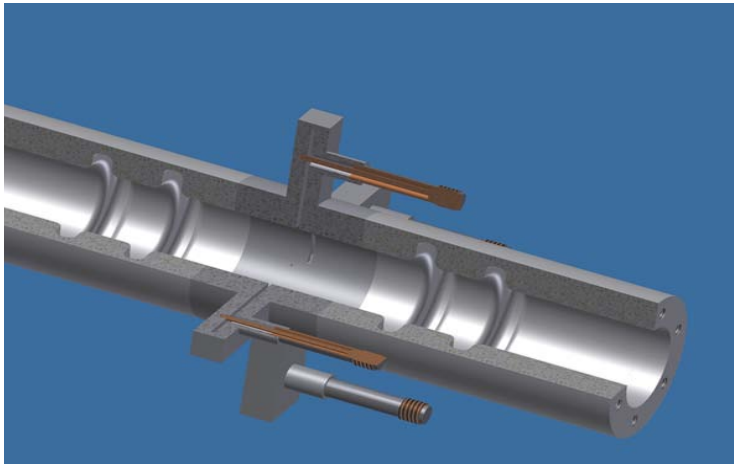
Latency contstrained by the beam TOF through the facility from TL1 to TL2 : 380 ns



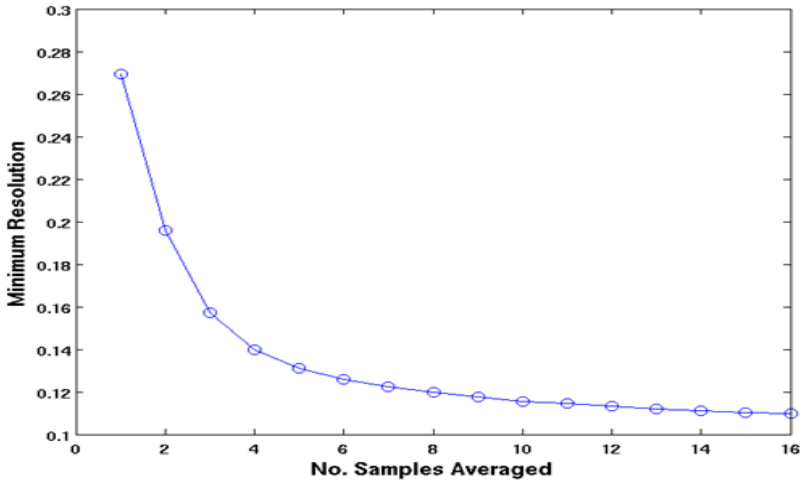
Phase Monitors

- Designed and built at INFN, Frascati
  - 12 GHz resonant cavities
    - 50 MHz bandwidth target
    - 0.1 degree (@ 12 GHz) phase resolution target
    - V. low coupling impedance to beam
  - Detection electronics produced by CERN





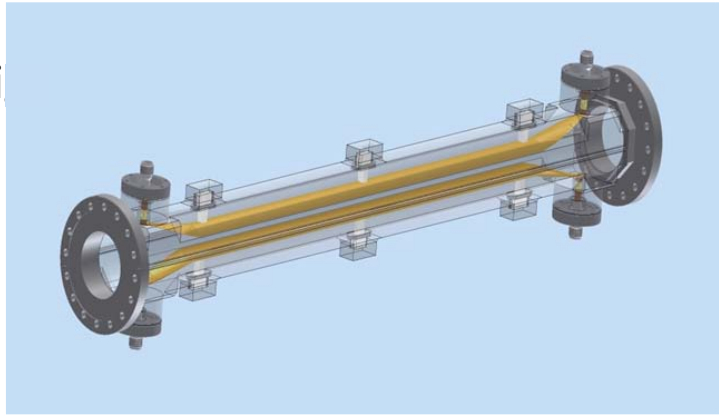
Resolution with averaging



Best achieved resolution ~ 0.14 degrees (single-point). 0.2 degrees more typical.

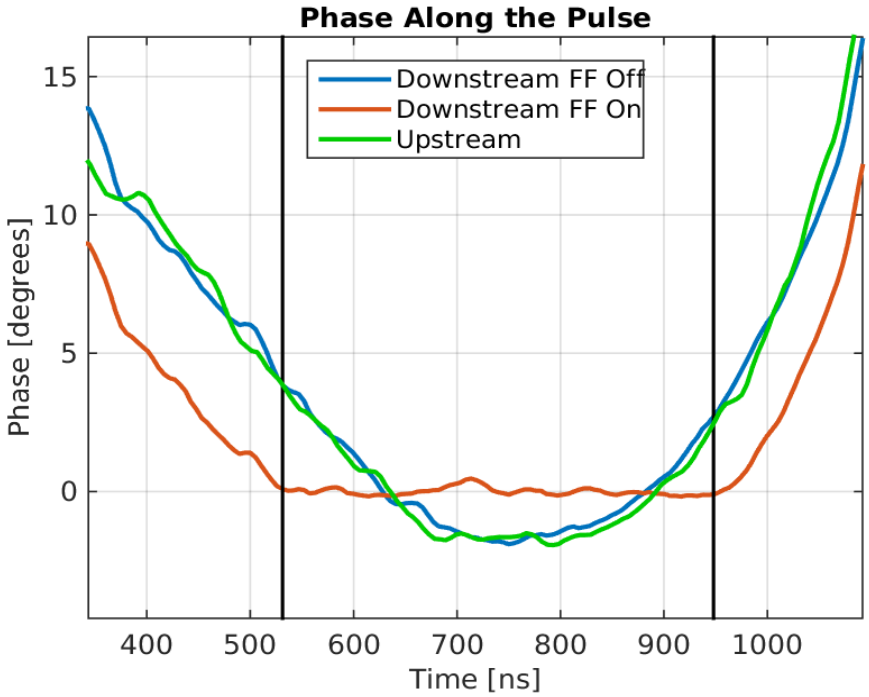
Amplifier / Kickers

- High-power, high-bandwidth amplifiers designed and built at JAI, Oxford
  - 65 kW nominal peak power
  - 1.2 us pulsed operation (unrestricted performance over ~400 ns portion of pulse)
  - Output droop limited to 10% across full pulse
  - > 50 MHz bandwidth (slew rate limited for large changes in drive)
- Kickers (INFN, Frascati)
  - 2 x ~1m long stripline kickers based on DAFNE desi
  - 1 mrad deflection for ~1.3 kV drive at 125 MeV

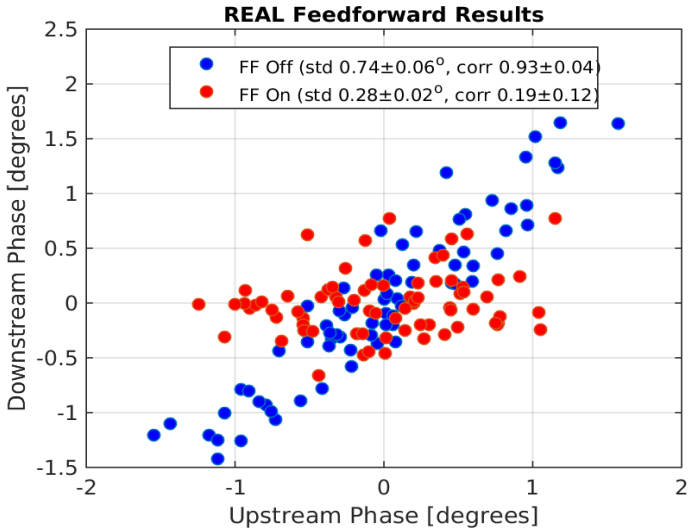


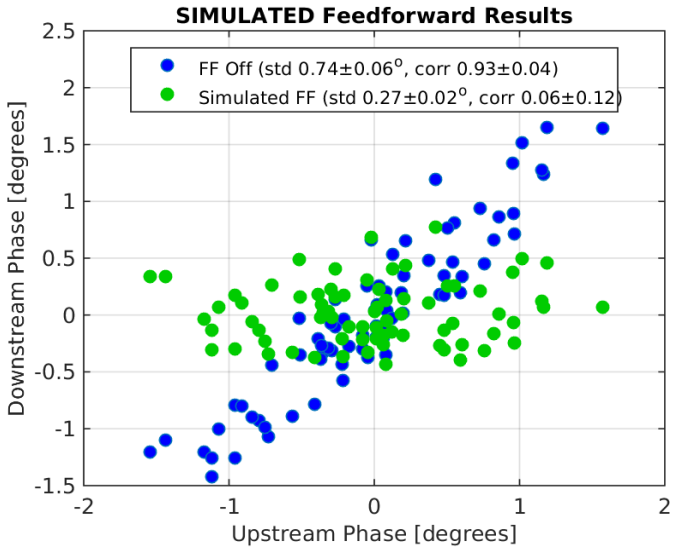
Combination of +/- 700 V drive and optics constriants in TL2 chicane give possible phase correction of +/- 5.5 degrees (at 12 GHz)

CTF3 PFF Latest Results



Stabilisation along the beam pulse: 0.26 +/- 0.01 (within operational range of correction) from 1.68 +/- 0.02 degrees at 12 GHz.





Summary

- Custom FPGA-based digital signal processor/feedback controller
  - Designed for low-latency applications
  - Nine ADC channels, clocked at up to 400 MHz, and 4 DACs
  - Standalone DAQ developed in LabVIEW with EPICs integration
- Position feedback systems at ATF2:
  - Upstream stripline BPM based 2-phase system, with to ~300 nm measurement precision
  - Achieved factor 3 correction, down to ~500 nm (resolution limited), witnessed ~30 m downstream in final-focus line
  - Surpassed goals for ILC!
- Phase-feedforward for CLIC/CTF3:
  - High-bandwidth phase stabilisation system for CLIC, using 2 kickers in TL2 line at CTF3
  - Phase monitor resoltion demonstrated to be below 0.2 degrees (0.14 degrees, best)
  - Correction of 0.26 degrees demonstrated both on pulse-pulse and intra-pulse phase jitter.

Acknowledgements

Thanks to all out colleagues and collaborators at KEK-ATF, CERN-CTF3, INFN Frascati, and the ATF2 Collaboration.

Muito obrigado!