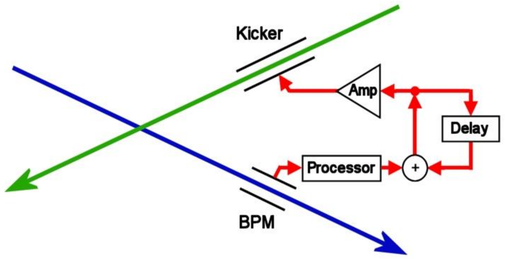
The FONT5 prototype ILC intra-train feedback system at ATF2

R. Apsimon, D. Bett, P.N. Burrows, G.B. Christian, B. Constance, C. Perry, J. Resta Lopez

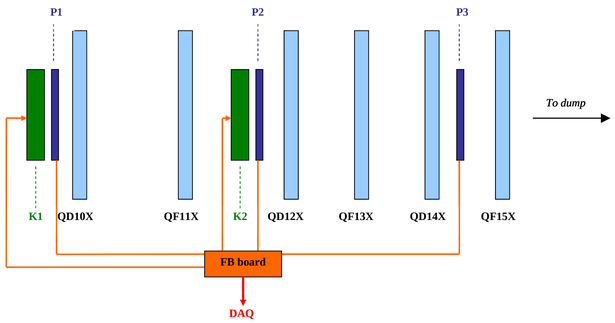
John Adams Institute, Oxford University, UK

Linear Collider intra-train IP feedback concept:

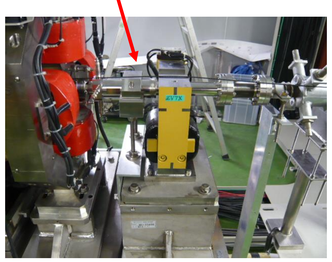


Detect position offset of incoming bunches early in train. Calculate correction and apply with kicker to later bunches

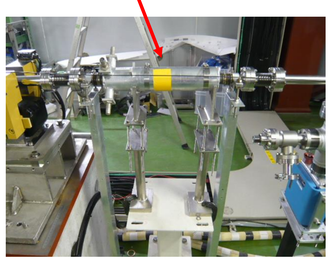
FONT5 digital prototype at KEK ATF2:



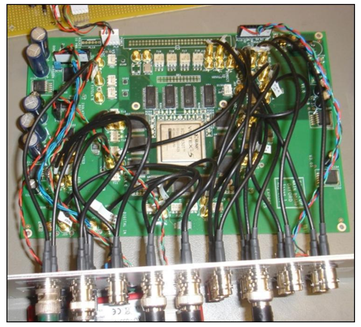
BPM P1



Kicker K1



Digital feedback processor:



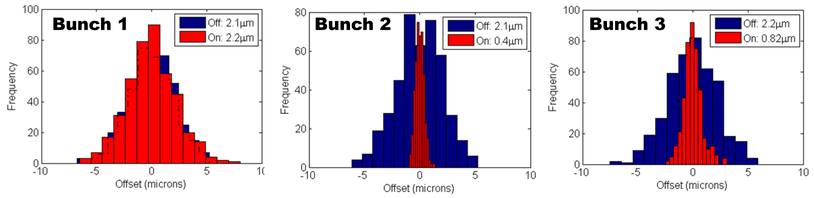
Xilinx Virtex5 FPGA

Clocked at 357 MHz phase-locked to beam

9 ADC input channels (TI ADS5474)

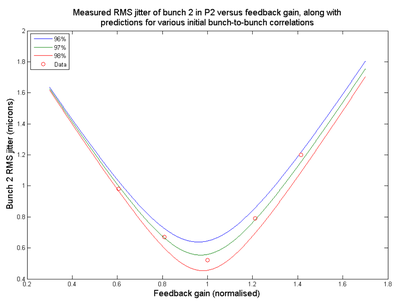
4 DAC output channels (AD9744)

Beam test results: single loop

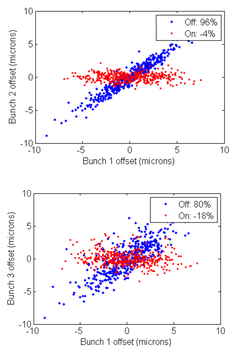


Jitter reduced by factor of 5

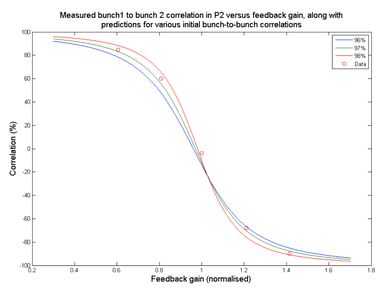
Jitter vs. FB loop gain



Performance of FB: removes correlations between bunches

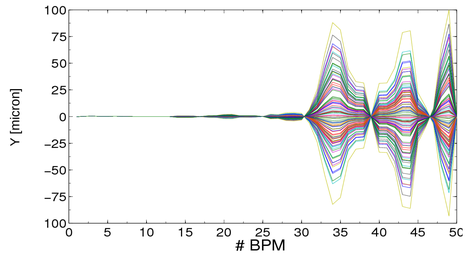


Bunch correlations vs. FB loop gain

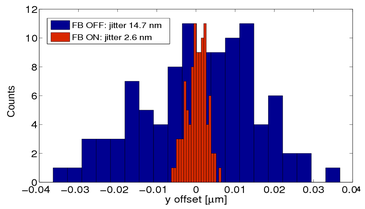


Extrapolation to ATF2 IP single loop:

Simulated propagation of 400nm jitter:

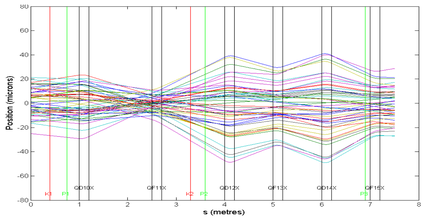


Jitter at IP:

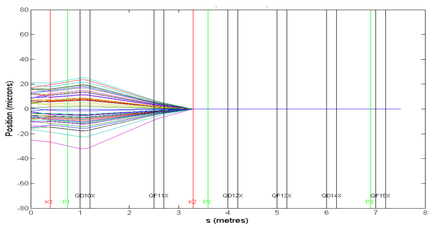


Extrapolation to ATF2 IP coupled loops:

Feedback off (simulation):



Feedback on (simulation):



Preliminary beam test results: coupled loops