NANOSECOND-LATENCY SUB-MICRON RESOLUTION STRIPLINE BEAM POSITION MONITOR SIGNAL PROCESSOR FOR CLIC

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Abstract

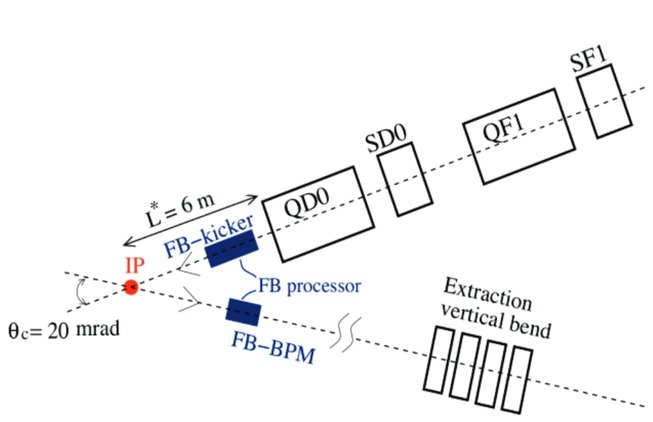
A high-resolution, low-latency stripline beam position monitor (BPM) signal processor has been developed for use in an intra-train feedback system for the Compact Linear Collider (CLIC). The processor was designed to have extremely low latency of order nanoseconds and a target position resolution of order 1 micron. The processor consists of a pair of diodes to form the difference and sum of a pair of stripline BPM inputs with microstrip filters to reduce out-of-band noise. The assembled prototype was optimized for use with the electron beam in the extraction line of the Accelerator Test Facility at the High Energy Accelerator Research Organization (KEK) in Japan but the underlying design is readily scaleable to a higher frequency response relevant for CLIC. A latency of 3 ns was measured in a testbench setup. We report the results of performance tests with beam in which the position resolution was measured to be c. 325 nm.

Introduction

CLIC IP feedback

In order to maintain the CLIC luminosity to within a few percent of the design value, intra-train feedback is required to provide sub-nanometre beam stabilisation. The CLIC trains are 156-176 ns long and consequently there are significant latency challenges associated with intra-train feedback [1]. The feedback latency determines how many iterations of feedback are possible within a single train, which in turn limits the luminosity recovery.

The CLIC intra-train feedback system (shown right) has a BPM and processor downstream of the IP to measure the deflected beam and a kicker and amplifier upstream of the IP for beam correction. The beam measurement and correction are applied to opposing beams so as to reduce the latency from signal propagation.



CLIC interaction region (3 TeV baseline design) showing the IP feedback BPM, BPM processor and kicker [2].

Processor requirements

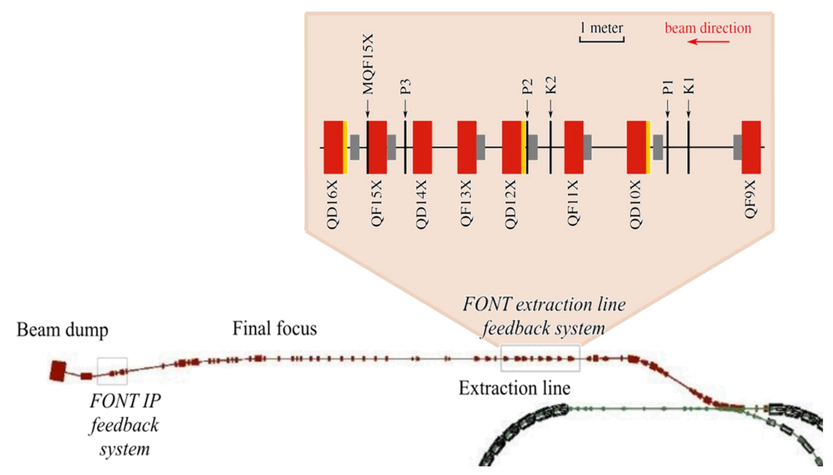
- Low-latency
- Radiation-hard
- Operates in a high magnetic field
- Simple
- Reliable
- Micron-level resolution

ATF2 setup

The diode processor was implemented at the Accelerator Test Facility, ATF2 (KEK, Japan) on the outputs of stripline BPM `P1' in the FONT extraction line feedback system (shown below). The ATF2 bunch charge (~1 nC) is comparable to the CLIC charge of 0.6 nC for the 3 TeV baseline design. BPMs P2 and P3 had conventional FONT processors [3]. The output from the processors were digitised on FONT5A boards [2].

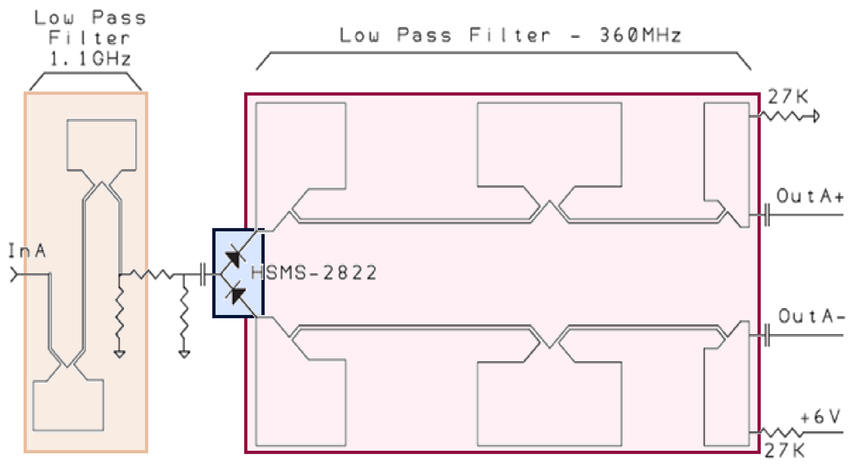
The ATF2 was configured with single bunch trains, whereas for CLIC there would be trains of 312-354 bunches. Problems are not expected when scaling to longer trains.

The P1 output peaks at 700 MHz compared with the 2 GHz CLIC repetition rate but the prototype was designed to be scaleable to the higher frequency CLIC signals.



Schematic of the ATF2 extraction line with FONT system highlighted, showing BPMs P1, P2 and P3 and kickers K1 and K2 [4].

Processor design



Schematic of the components of the diode processor required for CLIC, including diode detectors (blue) and 1.1 GHz and 360 MHz LPFs.

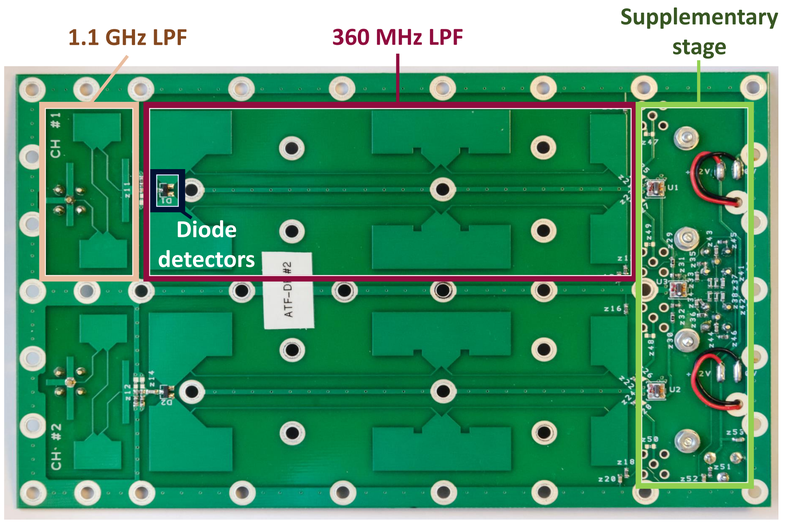
The processor (shown left) comprises:

- **a diode detector** to measure the signal amplitude from each electrode of the stripline BPM
- **a 1.1 GHz Low Pass Filter (LPF)** to smooth the sharp peaks in the BPM signals so as not to damage the diodes
- **a 360 MHz LPF** to reduce AC components introduced by the high-frequency CLIC bunch repetition rate

The processor outputs are via two ZX60-4016E amplifiers.

Supplementary stage

For the ATF2, a **supplementary stage** of processing (see right) is required to interface the diode processor and the FONT5A board used for digitisation. 180° combiners provide the sum and difference of the two electrode signals, a further LPF is used to broaden the pulse and an amplifier matches the processor output to the digitiser sensitivity.

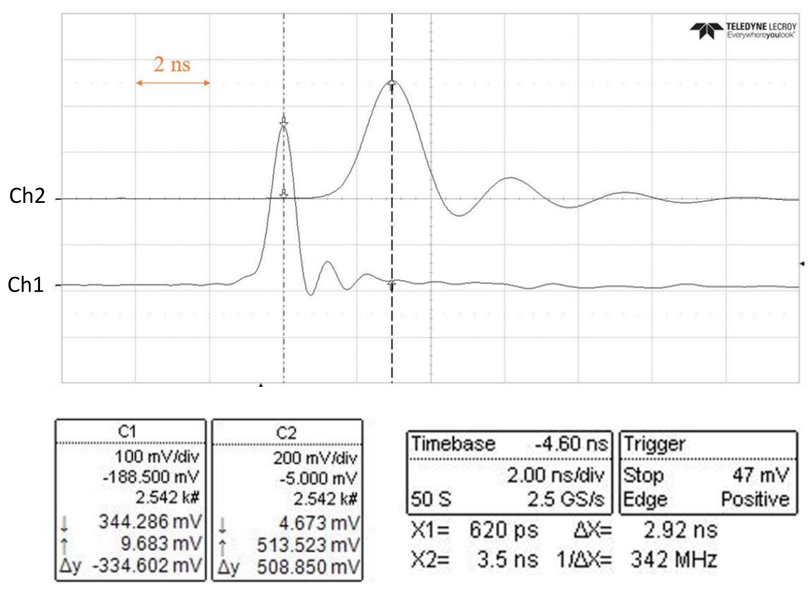


Photograph of the diode processor showing 1.1 GHz LPFs, diode detectors, 360 MHz LPFs and supplementary components.

Latency

With a CLIC bunch spacing of 0.5 ns it is critical to minimise the latency of a BPM processor used for intra-train feedback [1]. The diode processor tested at the ATF2 includes the processor components relevant for CLIC and also supplementary components to make the processor compatible with the ATF2 FONT system.

The full processor was measured to have a latency of ~3 ns, which would be expected to scale to ~1 ns when removing the components which were specific to ATF2 operation.



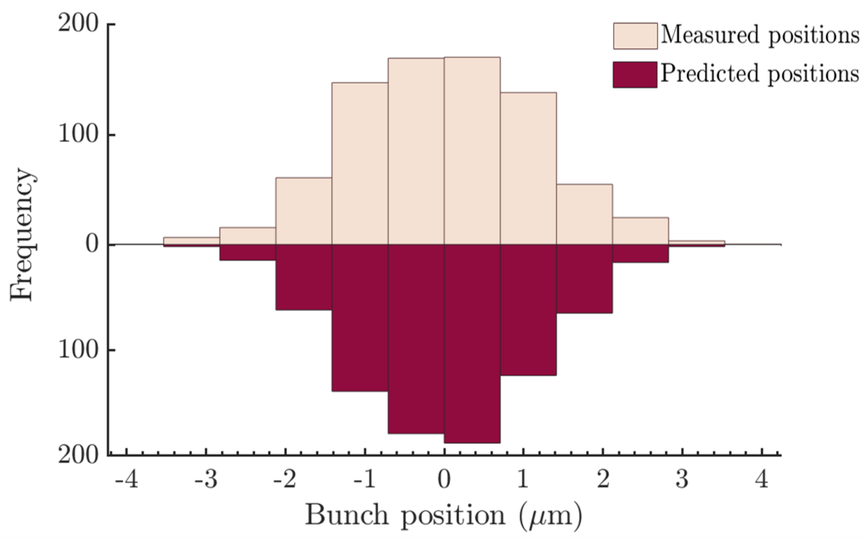
Oscilloscope waveforms from a testbench setup without (Ch1) and with (Ch2) the diode processor.

Resolution

To estimate the resolution, the *measured* bunch positions at P1 ($y^{\text{meas.}}$) were compared with the *predicted* bunch positions ($y^{\text{pred.}}$) for many consecutive triggers. The resolution σ_{P1} of the system is defined in terms of the resolutions of P2 and P3 (σ_{P2}, σ_{P3}) as

$$\sigma_{P1} = \sqrt{\text{std}\left(y_{\text{P1}}^{\text{meas.}} - y_{\text{P1}}^{\text{pred.}}\right)^2 - \text{A}\sigma_{P2}^2 - \text{B}\sigma_{P3}^2}.$$

By fitting for the coefficients A and B, and using previously measured values, $\sigma_{P2} = \sigma_{P3}$ =200 nm [5], the diode processor was estimated to have a resolution of ~325 nm. The distributions of $y_{\text{P1}}^{\text{meas.}}$ and $y_{\text{P1}}^{\text{pred.}}$ are shown below.



Distributions of measured and predicted bunch positions at P1, with standard deviations of 1.16 μm and 1.10 μm respectively.

Conclusion

A prototype processor has been constructed, suitable to be used in a CLIC IP feedback system. The design is suitable for operation in high magnetic fields and is radiation-hard. The processor was implemented at the ATF2 and demonstrated to have a latency of 3 ns which is expected to scale to ~1 ns for CLIC. The stripline BPM and processor setup was estimated to have a resolution of ~325 nm.

Outlook

To scale up in frequency from ATF2 operation to CLIC, the filters would need to scale down in size by a factor of ~2 to reduce parasitic capacitance and inductance. The 1.6 mm FR4 board would be replaced by a ~0.8 mm RF substrate board. For CLIC, the processor outputs could be input into differential amplifiers on a custom GaAs Monolithic Microwave Integrated Circuit.

References

[1] M. Aicheler *et al.*, CLIC conceptual design report, CERN-2012-007, (2012)
[2] J. Resta Lopez, *et al., Journal of Instrumentation* vol. 5, P09007 (2010)
[3] R.J. Apsimon *et al*, Phys. Rev. ST Accel. Beams **18**, 032803 (2015)
[4] http://newsline.linearcollider.org/images/2008/20081002_dc_1.jpg
[5] N. Blaskovic Kraljevic *et al.*, in *Proc. IPAC'17*, paper TUPIK110, pp. 1979-1982

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