Abstract

A high-resolution, low-latency stripline beam position monitor (BPM) signal processor has been developed for use in an intra-train feedback system for the Compact Linear Collider (CLIC). The processor was designed to have extremely low latency of order nanoseconds and a target position resolution of order 1 micron. The processor consists of a pair of diodes to form the difference and sum of a pair of stripline BPM inputs with microstrip filters to reduce out-of-band noise. The assembled prototype was optimized for use with the electron beam in the extraction line of the Accelerator Test Facility at the High Energy Accelerator Research Organization (KEK) in Japan but the underlying design is readily scaleable to a higher frequency response relevant for CLIC. A latency of 3 ns was measured in a testbench setup. We report the results of performance tests with beam in which the position resolution was measured to be <2.35 mm.

CLIC IP feedback

In order to maintain the CLIC luminosity to within a few percent of the design value, intra-train feedback is required to provide sub-nanometre beam stabilisation. The CLIC trains are 156-176 m long and consequently there are significant latency challenges associated with intra-train feedback [1]. The feedback latency determines how many iterations of feedback are possible within a single train, which in turn limits the luminosity recovery. The CLIC intra-train feedback system (shown right) has a BPM and processor downstream of the IP to measure the deflected beam and a kicker and amplifier upstream of the IP for beam correction. The beam measurement and correction are applied to opposing beams so as to reduce the latency from signal propagation.

Processor requirements

- Low-latency
- Radiation-hard
- Operates in a high magnetic field
- Simultaneous measurement and correction
- Reliable
- Microin-level resolution

The processor (shown left) comprises:

- a diode detector to measure the signal amplitude from each electrode of the stripline BPM
- a 1.1 GHz Low Pass Filter (LPF) to smooth the sharp peaks in the BPM signals so as not to damage the diodes
- a 360 MHz LPF to reduce AC components introduced by the high-frequency CLIC bunch repetition rate

The processor outputs are via two X60-4016G amplifiers.

Supplementary stage

For the ATF2, a supplementary stage of processing (see right) is required to interface the diode processor and the FONTSA board used for digitisation. 180° combiners provide the sum and difference of the two electrode signals, a further LPF is used to broaden the pulse and an amplifier matches the processor output to the digitiser sensitivity.

Latency

With a CLIC bunch spacing of 0.5 ns it is critical to minimise the latency of a BPM processor used for intra-train feedback [1]. The diode processor tested at the ATF2 includes the processor components relevant for CLIC and also supplementary components to make the processor compatible with the ATF2 FONT system. The full processor was measured to have a latency of ~3 ns, which would be expected to scale to ~1 ns when removing the components which were specific to ATF2 operation.

Resolution

To estimate the resolution, the measured bunch positions at P1 (y\text{meas}^P) were compared with the predicted bunch positions (y\text{pred}^P) for many consecutive triggers. The resolution σ_y^P of the system is defined in terms of the resolutions of P2 and P3 (σ_y^P, σ_y^P) as

\[ σ_y^P = \sqrt{σ_y^{P1} - \frac{y_{\text{meas}}^P - y_{\text{pred}}^P}{2}} + \sigma_y^{P2} + \sigma_y^{P3} \]

By fitting for the coefficients A and B, and using previously measured values, σ_y^P = 200 nm [5], the diode processor was estimated to have a resolution of <325 mm. The distributions of y\text{meas}^P and y\text{pred}^P are shown below.

Conclusion

A prototype processor has been constructed, suitable to be used in a CLIC IP feedback system. The design is suitable for operation in high magnetic fields and is radiation-hard. The processor was implemented at the ATF2 and demonstrated to have a latency of 3 ns which is expected to scale to ~1 ns for CLIC. The stripline BPM and processor setup was estimated to have a resolution of ~325 nm.

Outlook

To scale up in frequency from ATF2 operation to CLIC, the filters would need to scale down in size by a factor of ~2 to reduce parasitic capacitance and inductance. The 1.6 mm FR4 board would be replaced by a ~0.8 mm RF substrate board. For CLIC, the processor outputs could be input into differential amplifiers on a custom GaAs Monolithic Microwave Integrated Circuit.

References