DESIGN, TESTING AND PERFORMANCE RESULTS OF A HIGH-RESOLUTION, BROAD-BAND, LOW-LATENCY STRIPLINE BEAM POSITION MONITOR SYSTEM

N. Blaskovic Kraljevic, D. R. Bett, T. Bromwich, P. N. Burrows, G. B. Christian, M. R. Davis, C. Perry,
John Adams Institute, Oxford, UK

Abstract

A high-resolution, low-latency beam position monitor (BPM) system has been developed for use in particle accelerators and beamlines that operate with trains of particle bunches with bunch separations as low as several tens of nanoseconds, such as future linear electron-positron colliders and free-electron lasers. The system was tested with electron beams in the extraction line of the Accelerator Test Facility at the High Energy Accelerator Research Organization (KEK) in Japan. The fast analogue front-end signal processor is based on a single-stage RF down-mixer. The processor latency is 15.6 +- 0.1 ns. A position resolution below 300 nm has been demonstrated for beam intensities of around 1 nC, with single-pass beam.

INTRODUCTION

A number of in-construction and proposed future particle accelerator designs feature trains of particle bunches with bunch-separation intervals in the ranges of nanoseconds to tens or hundreds of nanoseconds. For example, the International Linear Collider (ILC) design [1] calls for bunch trains comprising thousands of bunches separated in time by around 500 ns with a train repetition frequency of 5 Hz; the Compact Linear Collider (CLIC) design [2] specifies bunch trains comprising several hundred bunches separated in time by around 0.5 ns, with a train repetition frequency of 50 Hz. Free-electron lasers based on similar accelerating technologies as ILC and CLIC will have similar bunch-train time structures, such as the European XFEL [3], which will have a minimum bunch spacing of 200 ns and a repetition rate of 10 Hz. Beam control at such facilities calls for beam position monitors (BPMs) that can resolve bunches on an intra-train (ideally bunch-by-bunch) timescale, with submicron position resolution in single-pass mode. The design of such a BPM system is presented here.

FONT5 SYSTEM AT ATF2

The system was developed by the Feedback on Nanosecond Timescales (FONT) group [4] and it was deployed, commissioned and tested at the Accelerator Test Facility (ATF) [5] at KEK. The layout of the BPMs is shown in more detail in Fig. 1. The design goal for the FONT5 system is to stabilize the vertical beam position to the 1 μm level at the entrance to the final-focus system. This requires BPMs capable of resolving bunches separated in time by around 100 ns, and with a position resolution at the submicron level. For tests of the FONT5 system the ATF is operated in a mode whereby a train of two or three bunches is extracted from the damping ring and sent down the ATF2 beam line. The bunch separation is determined by the damping ring fill pattern and typically is chosen to be between 140 ns and either 154 ns (3-bunch mode) or 300 ns (2-bunch mode).

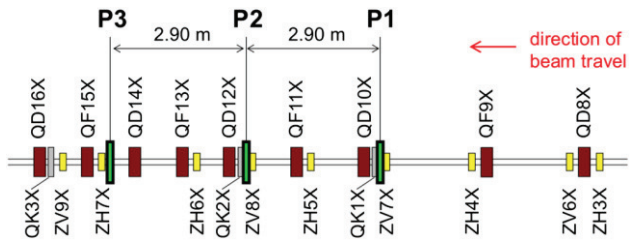

Figure 1: Layout of the FONT5 BPMs (P1, P2 and P3) in the ATF2 extraction line; quadrupole ("Q") and dipole corrector ('Z') magnets are indicated.

The FONT5 BPM system (Fig. 2) consists of three stripline BPMs (Fig. 3) each of which is instrumented with an analogue processor, and a custom multichannel digitizer. Stripline BPMs were used due to their inherently fast, broadband response and capability to resolve bunches with the required time resolution. In the FONT5 system, only the vertical plane of the BPMs is routinely instrumented.

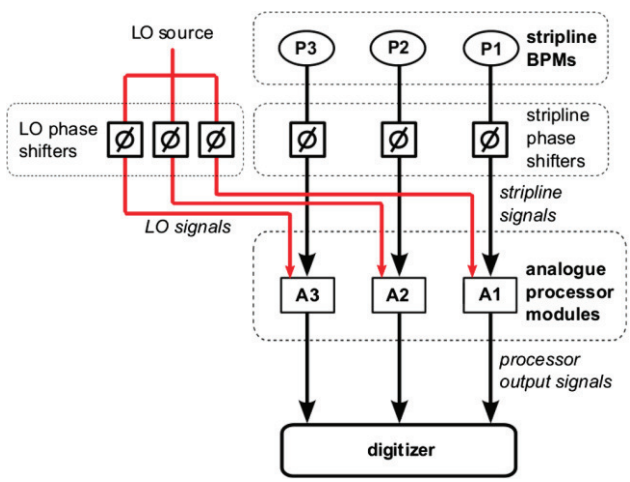

Figure 2: Schematic of the FONT5 BPM system. For each BPM, a phase shifter is used on one of the stripline signals to adjust the relative path lengths of the two input signals at the BPM processor, and another phase shifter is used to adjust the phase of the LO signal at each processor.

ISBN 978-3-95450-168-7

The FONT5 analogue processors' (Fig. 4) function [6] is to deliver the stripline pickoff-pair difference and sum signals in a form that can be easily recorded by the digitizer for calculation of the position-dependent, beam charge-independent ratio of the two. Ten processors were built and are used in beam operations at ATF2. A single BPM processor can be used to process the beam position data in either the horizontal or vertical plane; from here on only the vertical plane is considered. The BPM processor outputs are digitised by a custom digital feedback processor board (Fig. 5). The board has nine analogue signal input channels digitised using ADCs with a maximum conversion rate of 400 MS/s, and two analogue output channels formed using DACs, which can be clocked at up to 210 MHz. The digital signal processing is based on a Xilinx Virtex5 FPGA. The FPGA is clocked with a 357 MHz source derived from the ATF master oscillator and hence locked to the beam. The ADCs are clocked at 357 MHz.

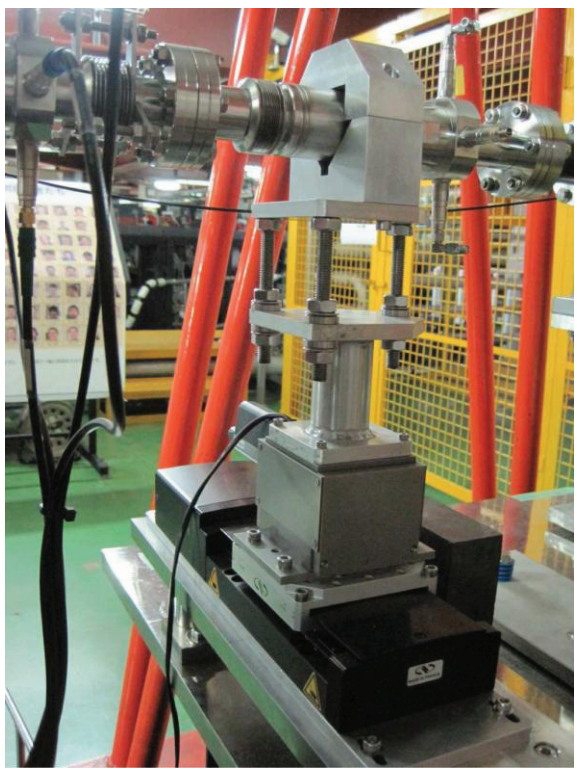

Figure 3: Photograph of FONT5 stripline BPM P3 and its mover in the ATF2 beam line.

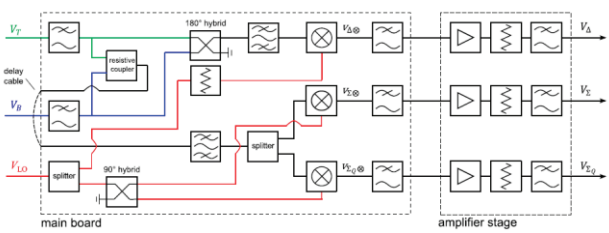

Figure 4: Schematic diagram illustrating the structure of the FONT5 analogue processor.

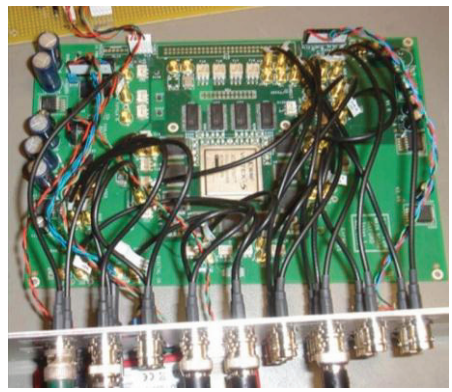

Figure 5: FONT5 digital feedback board.

PROCESSOR LATENCY

The latency of the processor is defined to be the time interval between the arrival of the stripline signals at the inputs and the peak of the signals at the outputs. One of the principal design goals was that the latency should be low, while providing baseband output pulses that are amenable to convenient digitization. The latency was measured by using a test bench to provide realistic beam-proxy input signals and observing on an oscilloscope the arrival time of the processed output signal (Fig. 6). Subtracting from this the time of arrival at the oscilloscope of the input when the processor is bypassed, the processor latency before the amplifier stage was found to be 10.4+-0.1 ns, and 15.6+-0.1 ns including the amplifier stage (Fig. 6).

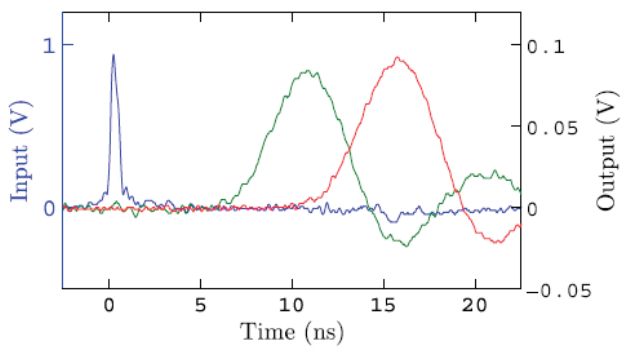

Figure 6: Input beam proxy signal (blue, left-hand scale) and processor output difference signal before the amplifier stage (green, right-hand scale, with factor 5 multiplication), and after the amplifier stage (red, right-hand scale), vs time (ns). The amplifier stage delays the output signal by an additional 5.2 ns.

SYSTEM PERFORMANCE

The range of linear response is defined to be the range over which the system responds linearly to a change in beam position. A nonlinear response is expected if the input signal to a mixer (Fig. 4) is large enough to cause its output to saturate. Saturation will be avoided if the mixer RF input signal level is small compared with the design LO input signal level, ~7 dBm. For optimum resolution, the stripline BPM signals can be attenuated to ensure that

ISBN 978-3-95450-168-7

for the nominal beam charge (~1 nC) the sum-channel signal level is comfortably below the mixer saturation point. The processor output is then expected to be linear for $|y| \lesssim 400$ μm. As an illustration, Fig. 7 shows the raw beam position measured in BPM P3 as a function of the vertical BPM position. The measurements visibly deviate from linearity for beam positions more than 500 μm from the electrical zero point; within this range, the deviation from linearity is less than 2%. A larger range could be obtained with the system described here by increasing the attenuation of the stripline signals input to the processor, although this would degrade the position resolution.

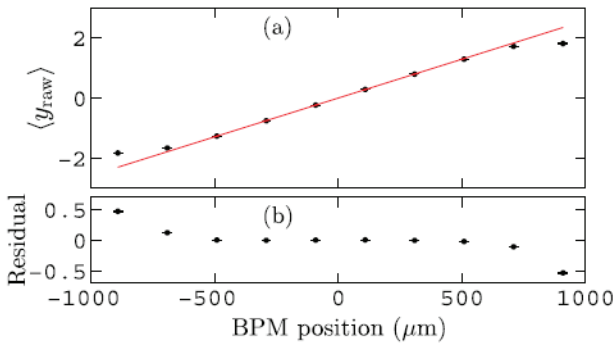

Figure 7: (a) Raw beam position vs vertical BPM position. 50 beam pulses are averaged at each setting; the red line is a linear fit to the central four data points. (b) Residual of the data with respect to the fitted line.

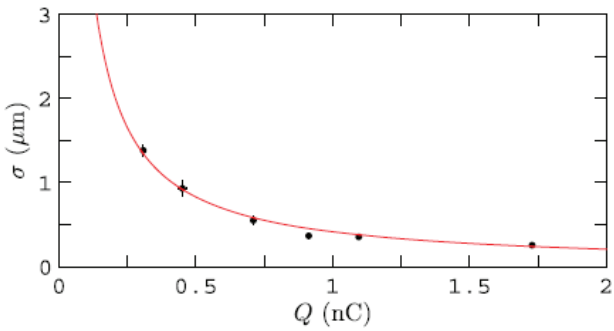

Figure 8: Position resolution vs beam charge (Q); the red line shows a fit of the function $\sigma = p/Q$, where p is a parameter. Note that for this data set the raw stripline signals were attenuated by 6 dB in order to handle the very large signal levels at the higher charge settings.

The resolution of the system is determined by comparing the beam position measured in one BPM with the position predicted at that BPM on the basis of the beam positions measured in the other two BPMs. Assuming that the three BPMs have the same resolution, σ, these residuals yield a resolution estimate, for a centered beam with a bunch charge of approximately 1 nC, of σ = 291+-10 nm [7] which is world leading in terms of the position resolution obtained in stripline BPMs in single-pass beam mode. Such a level of performance is achieved routinely in beam operations. For comparison, a global least-squares fit can be performed to explicitly minimize σ. For the same data set this yields a value for the resolution of 262+-11 nm. As this method removes any correlated components of the BPM position data, and also allows for variation in the individual BPM scale factors, this result represents the minimum possible resolution that could, in principle, be attained, if for example any residual correlated effects were accounted for. In contrast, the value obtained using the beam line model better represents the actual minimum sensitivity attainable in a given position measurement. The value attained with the least-squares fit is consistent with that expected from the measured system noise.

Figure 8 shows the resolution for a data run which includes different beam charges. The charge dependence is as expected. This data was taken with 6 dB of stripline attenuation; comparable resolution could be achieved at half the charge with this attenuation removed.

CONCLUSIONS

The design and performance of a stripline BPM system based on an analogue signal processing scheme has been presented. The system was designed for low-latency operation and high resolution measurement of beam position. The latency of the analogue processing electronics was measured to be 15.6+-0.1 ns. The position resolution was measured to be 291+-10 nm for a beam of bunch charge approximately 1 nC. At this charge a linear range of $|y| < 500$ μm is observed, giving a dynamic range of ~60 dB. The resolution was found to scale with bunch charge and beam position in the expected manner. The measured performance is close to that expected from the measured system noise, and within a factor 3 of the theoretical noise limit of ~100 nm. For an ideal optimized implementation of this architecture, a factor 2 to 3 improvement in the resolution could, in principle, be achieved.

ACKNOWLEDGMENTS

We thank the KEK ATF staff for their outstanding logistical support and beam time and our ATF2 collaborators for their help and support. Financial support was provided by the UK Science and Technology Facilities Council, CERN contract KE1869/DG/CLIC, and the European Commission under the FP7 Research Infrastructures project EuCARD, Grant No. 227579.

REFERENCES

[1] C. Adolphsen et al., The ILC technical design report, volume 3: Accelerator, JAI-2013-001, 2013.
[2] M. Aicheler et al., CLIC conceptual design report, CERN-2012-007, 2012.
[3] M. Altarelli et al., The European X-Ray Free-Electron Laser: Technical Design Report, DESY 2006-097, 2006.
[4] http://www-pnp.physics.ox.ac.uk/~font/index.html.
[5] G.R. White et al., Phys. Rev. Lett. **112**, 034802 (2014).
[6] R. J. Apsimon, D. Phil. thesis, University of Oxford, 2011.
[7] R.J. Apsimon et al., Phys. Rev. ST Accel. Beams **18**, 032803 (2015).