DEVELOPMENT OF A HIGH-RESOLUTION, BROAD-BAND, STRIPLINE BEAM POSITION MONITORING SYSTEM

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Abstract

A low-latency, sub-micron resolution stripline beam position monitoring system has been developed and tested with beam at the KEK Accelerator Test Facility, where it has been used as part of a feedback system for beam stabilisation. The fast analogue front-end signal processor is based on a single-stage down-mixer and is combined with an FPGA-based system for digitisation and feedback control. A resolution as low as 400 nm has been demonstrated for beam intensities of ~1 nC, with single-pass beam. The latest results of recent modifications to balance the input path lengths to the processor will be discussed. These modifications compensate for the inherent phase sensitivity of the processors, and hence improve the intrinsic resolution, without the need for offline correction. Modifications to the FPGA firmware will also be described, to allow for flexible operation with variable system-synchronous data acquisition at up to 400 MHz, with up to nine data channels of 13-bit width, and a nominal record length of 1 kS/channel/pulse (extensible to a total record length of 120 kS per pulse, for example, for use with long bunch trains or wide-band multi-turn measurements in storage rings).

INTRODUCTION

The designs for the International Linear Collider (ILC) [1] and the Compact Linear Collider (CLIC) [2] require beams stable at the nanometre level at the interaction point (IP). In support of this, the goal of the ATF2 collaboration based at KEK, Japan is to achieve position stability at the notional IP of approximately 2 nm. To this end, the Feedback On Nanosecond Timescales (FONT) project [3] operates a position and angle feedback system [4] in the extraction line of the Accelerator Test Facility (ATF) [5]. In order to achieve the required level of position stability at the IP, the FONT feedback system needs to stabilise the beam to 1 micron at the entrance to the final focus system; this requires a BPM processing scheme capable of delivering position signals accurate to the sub-micron level on a timescale of the order of 10 ns.

The FONT beam position monitoring system makes use of 3 12~cm stripline BPMs (Figure 1), which are located in the diagnostics section of the ATF extraction line (FONTP1, FONTP2, FONTP3). The BPMs are connected to specially developed analogue processing electronics [6] in order to deliver appropriate position signals to an FPGA-based digital hardware module [7] that digitizes the signals and returns the sampled data to a computer where they are logged.

Figure 1: Stripline BPM FONTP1 at the ATF.

BPM PROCESSOR DESIGN

A schematic of the processor module is shown in Figure 2. The operation is as follows: the top (V_A) and bottom (V_B) stripline BPM signals are subtracted using a 180-degree hybrid to form a difference (Δ) signal and are added using a resistive coupler to form a sum signal. The resulting signals are then band-pass filtered and down-mixed with a 714 MHz local oscillator (LO) signal phase-locked to the beam before being low-pass filtered and amplified using 16dB low-noise amplifiers. The hybrid, filters and mixer were selected to have latencies of the order of a few nanoseconds in order to yield a total processor latency of 10ns [8].

The phasing of the LO with respect to the beam signal is maintained using an adjustable phase shifter on the LO input to the processor. In the sum channel, a 90-degree hybrid is used to downmix the raw sum signal with two orthogonal phases of the LO, producing an in-phase sum signal (Σ) and quadrature-phase sum signal (Σ_Q). The phase of the difference channel is accurately matched to that of the in-phase sum signal via a custom loopback cable in the sum channel. Hence the optimal phasing of both the Σ and Δ signals is achieved by minimising the Σ_Q signal.

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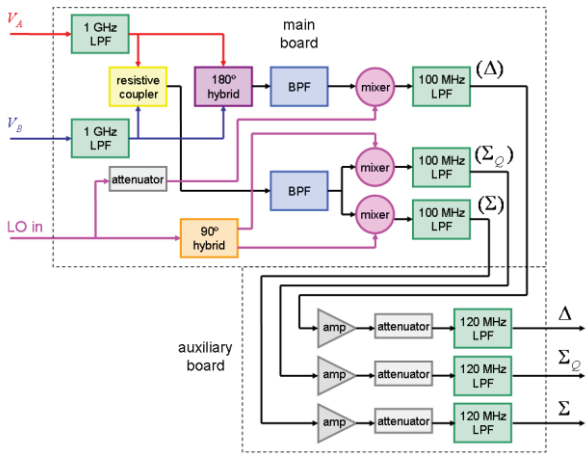

Figure 2: FONT analogue signal processor design.

The three output signals (Σ, Δ, Σ_Q) are digitized using analogue-to-digital converters (ADCs) on the FONT5 digital board [7], capable of converting at up to 400 MHz with 14-bit resolution. Low-noise amplifiers, with a gain of 16 dB, built into the processor modules are used to boost the input levels to just above the digitiser noise floor, and hence maximise the dynamic range of the measurement system. The ADCs, and sampling logic of the FPGA, are clocked in a system-synchronous mode at 357 MHz, this being a convenient frequency derived from the machine RF. The ADC clock may be delayed in increments of 70 ps to allow sampling at the exact time the bunch arrives. There are nine ADCs in total and so a single board is able to fully record the data from three BPMs.

The difference signal is a function of both the beam position and intensity. For this reason, in order to determine the position, the difference-on-sum method is used, thereby immunising against charge fluctuations. For an individual BPM, the resolution, σ_y, will be limited by the measurement noise, σ_Δ and σ_Σ, as given by the equation, below, where y and Σ are the absolute beam position and stripline sum signal, respectively. The resolution will vary linearly with position offset and inversely with intensity:

$$\sigma_y^2 = {}^1\!/_{\Sigma^2}\left[\sigma_\Delta^2 + y^2\sigma_\Sigma^2\right]$$

The phase of the LO with respect to the beam (φ_{LO}) in radians is equal to the ratio Σ_Q/Σ for small deviations and is subject to both jitter and a slow sinusoidal oscillation, the combined effect of which is an RMS variation of about 0.5 degree (Fig. 3). The dominant contribution to the phase jitter has been shown to be due to the synchrotron oscillation of the bunch with respect to the machine RF [8]. This variation of φ_{LO} manifests itself as an apparent change in the measured position of the beam, (Fig. 4) and this can be compensated as described below (see also [9]).

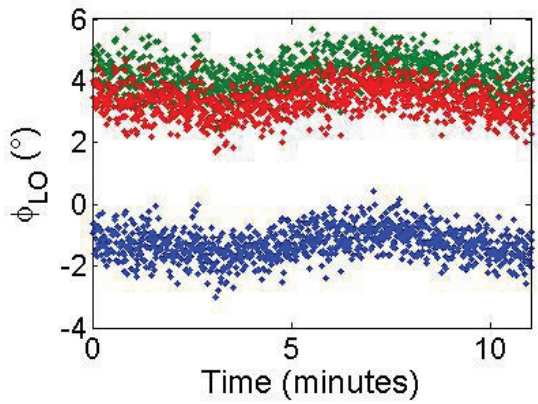

Figure 3: Stability of the LO phase as measured by the processor on FONTP1 (blue), FONTP2 (green) and FONTP3 (red).

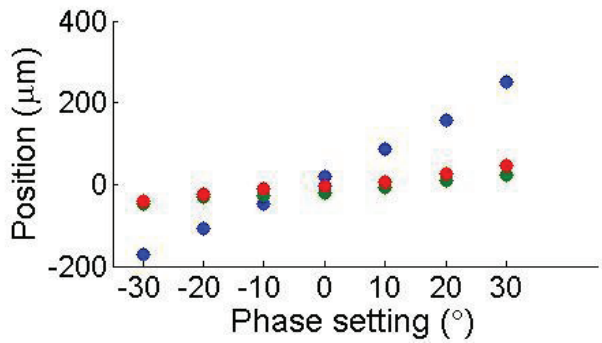

Figure 4: Effect on measured position of a change in the LO phase for FONTP1 (blue), FONTP2 (green) and FONTP3 (red).

PERFORMANCE

The BPMs (FONTP1, FONTP2, and FONTP3) are seated on a two-axis (x-y) mover system with a range of motion of several mm. This allows each BPM's electrical centre to be positioned on the beam axis, and also allows each BPM to be usable, if desired, within a limited dynamic range, without the need to steer the beam through the BPM using upstream dipole magnets. The BPMs are calibrated by scanning the BPM mover and comparing the change in processor output to the known displacement of the BPM.

Figure 5 shows an example of a BPM mover scan, illustrating the dynamic range of the processor. The linearity of the processor is determined by the level at which the mixer will saturate. The attenuation in the sum channel of the BPM processor is set so that the nominal beam intensity of 0.5 x 10^{10} e^- corresponds to a sum signal just below mixer saturation, hence optimising resolution and dynamic range. This results in a linear region to $\Delta/\Sigma \approx \pm 1$, corresponding to ~400 μm, over which the calibration constant is obtained.

BPM resolution is calculated from the system of three BPMs by removing the contribution from the LO phase, performing drift subtraction and then using the measurements from two of the BPMs to predict the

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position in the third. It is assumed that the three BPMs have similar resolution. The best result obtained to date is shown in Figure 6 which suggests the resolution of the combined system of BPMs FONTP1, FONTP2 and FONTP3 is 0.43 microns.

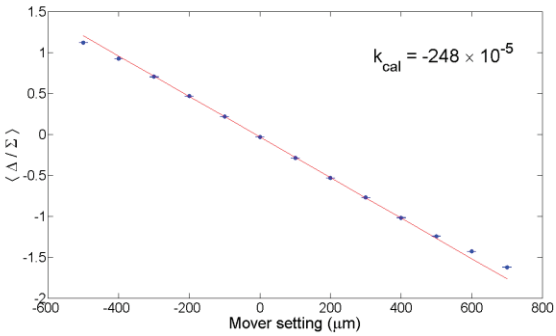

Figure 5: Example BPM calibration illustrating the dynamic range of the processor, showing Δ/Σ for each mover setting (blue) and linear fit to data (red). The calibration is obtained for the linear region where |Δ/Σ|<1.

FURTHER MODIFICATIONS

The sub-micron results shown in Fig.6, and reported on in [9], were obtained by subtracting offline the LO phase jitter contribution from the position data, on a shot-by-shot basis. For use in real-time feedback systems this correction must be taken into account online, in order to avoid introducing spurious noise back into the beam trajectories due to the apparent jitter in the measurement system. This correction can be done online on a shot-by-shot basis, in a similar way to the offline correction, or (and preferably) by minimising the inherent phase sensitivity of each individual processor.

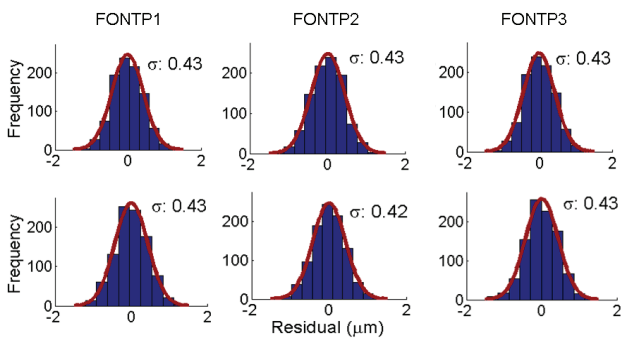

Figure 6: Histograms of residuals for BPMs FONTP1, FONTP2 and FONTP3 (blue) obtained by predicting the position using the transfer matrices (top) and by a least-squares fit to the other two positions (bottom); a Gaussian fit to the data is plotted in each case (red) and the width is given in microns.

The major contributing factor to the phase sensitivity comes from a path length imbalance to the 180-degree, difference-forming, hybrid. A relative difference in the path lengths to the hybrid will result in a quadrature-like residual in the difference signal measured, and any jitter between the LO phase and beam signal at the mixer will translate into a position jitter proportional to this path length imbalance. This imbalance is unique for every combination of stripline BPM and processor, and to correct the imbalance each processor is equipped with a pair of rotary phase shifters on the raw BPM inputs. One of these phase shifters is manually set to approximately match the path length of the other channel, and the second is controlled remotely so as to null the phase sensitivity of the BPM and processor combination in situ.

This has been tested on FONTP2 and FONTP3, the two striplines used as inputs for the real-time feedback system [4], and resolution results comparable to those in Fig. 6 are routinely demonstrated, without the need for offline phase compensation at FONTP2 and FONTP3.

Modifications have also been made to the data acquisition in the FPGA firmware, and associated software systems, to generalise the functionality for use in other applications or with similar stripline BPM processors designed for other facilities, with different timing parameters. The previous data acquisition system was designed around the timing parameters at ATF; for example, use of a 357 MHz clock for the sampling logic was assumed. The upgraded firmware will allow for flexibility in the data acquisition with a system clock in the range 200-400 MHz. The nominal record length for each of the nine data channels will be up to 1024 samples per channel per pulse; previously this was limited to a period corresponding to one revolution of the ATF damping ring (462 ns). This could be extended to up to 120 kS/pulse by allocating all available memory blocks on the FPGA to one particular channel, which could be useful for measurement and control of long trains of bunches or for high bandwidth measurements in storage rings.

REFERENCES

[1] http://www.linearcollider.org/cms/
[2] http://clic-study.web.cern.ch/CLIC-Study/
[3] www-pnp.physics.ox.ac.uk/~font/
[4] M.R. Davis et al, these proceedings.
[5] http://www-atf.kek.jp/atf/.
[6] R. Apsimon, DPhil thesis, University of Oxford (2011).
[7] B. Constance, DPhil thesis, University of Oxford (2011).
[8] G. B. Christian et al, Proceedings IPAC12, MOPPR064.
[9] D.R. Bett et al, Proceedings IPAC12, MOPPR065.