LATEST PERFORMANCE RESULTS FROM THE FONT5 INTRA-TRAIN BEAM POSITION AND ANGLE FEEDBACK SYSTEM AT ATF2

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Abstract

A prototype Interaction Point beam-based feedback system for future electron-positron colliders, such as the International Linear Collider, has been designed and tested on the extraction line of the KEK Accelerator Test Facility (ATF). The FONT5 intra-train feedback system aims to stabilize the beam orbit by correcting both the position and angle jitter in the vertical plane on bunch-to-bunch time scales, providing micron-level stability at the entrance to the ATF2 final-focus system. The system comprises three stripline beam position monitors (BPMs) and two stripline kickers, custom low-latency analogue front-end BPM processors, a custom FPGA-based digital processing board with fast ADCs, and custom kicker-drive amplifiers. The latest results from beam tests at ATF2 will be presented, including the system latency and correction performance.

INTRODUCTION

A number of fast beam-based feedback systems are required at the International Linear Collider (ILC) [1]. At the interaction point (IP) a very fast system, operating on nanosecond timescales within each bunchtrain, is required to compensate for residual vibration-induced jitter on the final-focus magnets by steering the electron and positron beams into collision. A pulse-to-pulse feedback system is envisaged for optimising the luminosity on timescales corresponding to 5 Hz. Slower feedbacks, operating in the 0.1 – 1 Hz range, will control the beam orbit through the Linacs and Beam Delivery System.

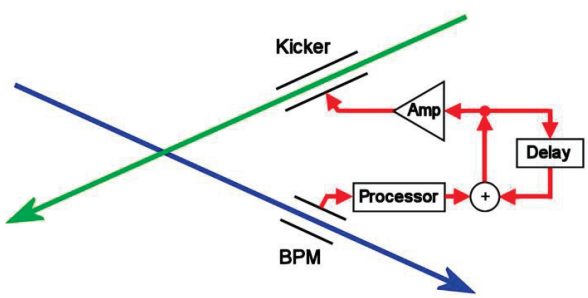

Figure 1: Schematic of IP intra-train feedback system with a crossing angle. The deflection of the outgoing beam is registered in a BPM and a correcting kick applied to the incoming other beam.

The key components of each such system are beam position monitors (BPMs) for registering the beam orbit; fast signal processors to translate the raw BPM pickoff signals into a position output; feedback circuits, including delay loops, for applying gain and taking account of system latency; amplifiers to provide the required output drive signals; and kickers for applying the position (or angle) correction to the beam. A schematic of the IP intra-train feedback is shown in Figure 1, for the case in which the beams cross with a small angle; the current ILC design incorporates a crossing angle of 14 mrad. Critical issues for the intra-train feedback performance include the latency of the system, as this affects the number of corrections that can be made within the duration of the bunchtrain, and the feedback algorithm.

We report the latest results on the development and beam testing of an ILC prototype system that incorporates a digital feedback processor based on a state-of-the-art Field Programmable Gate Array (FPGA) [2]. The use of a digital processor allows for the implementation of more sophisticated algorithms which can be optimised for possible beam jitter scenarios at ILC. However, a penalty is paid in terms of a longer signal processing latency due to the time taken for digitisation and digital logic operations. This approach is possible for ILC given the long, multi-bunch train, which includes parameter sets with c. 3000/6000 bunches separated by c. 300/150ns respectively. Initial results were reported previously [3].

FONT5 DESIGN

A schematic of the FONT5 feedback system prototype and the experimental configuration in the upgraded ATF extraction beamline, ATF2, is shown in Figure 2. Two stripline BPMs (P2, P3) are used to provide vertical beam position inputs to the feedback. Two stripline kickers (K1, K2) are used to provide fast vertical beam corrections. A third stripline BPM (P1) is used to witness the incoming beam conditions. Upstream dipole corrector magnets (not shown) can be used to steer the beam so as to introduce a controllable vertical position offset in the BPMs. Each BPM signal is initially processed in a front-end analogue signal processor. The analogue output is then sampled, digitised and processed in the digital feedback board. Analogue output correction signals are sent to a fast amplifier that drives each kicker.

ISBN 978-3-95450-115-1

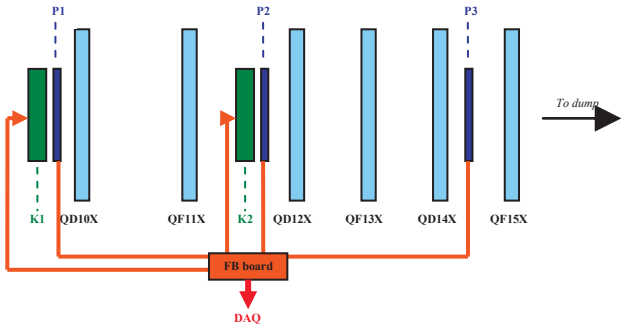

Figure 2: Schematic of FONT5 at the ATF2 extraction beamline showing the relative locations of the kickers, BPMs and the elements of the feedback system.

The ATF can be operated to provide an extracted train that comprises up to 3 bunches separated by an interval that is selectable in the range 140 - 300 ns. This provides a short ILC-like train which can be used for controlled feedback system tests. FONT5 has been designed as a bunch-by-bunch feedback with a latency goal of around 140ns, meeting the minimum ILC specification of c. 150ns bunch spacing. This allows measurement of the first bunch position and correction of both the second and third ATF bunches.

The design of the front-end BPM signal processor is described in [4]. The top and bottom (y) stripline BPM signals were added with a resistive coupler and subtracted using a hybrid, to form a sum and difference signal respectively. The resulting signals were band-pass filtered and down-mixed with a 714 MHz local oscillator signal which was phase-locked to the beam. The resulting baseband signals are low-pass filtered. The hybrid, filters and mixer were selected to have latencies of the order of a few nanoseconds to yield a total processor latency of 10ns [5,6].

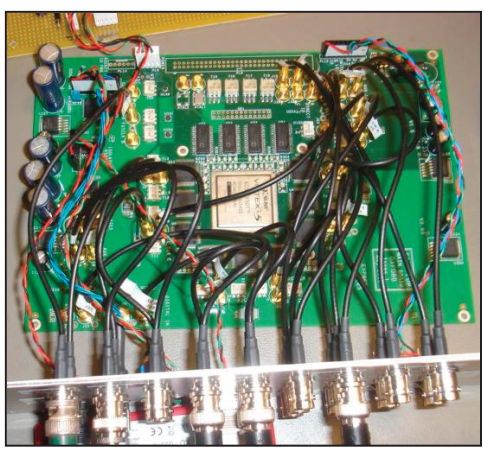

Figure 3: FONT5 digital feedback board.

The custom digital feedback processor board is shown in Figure 3. There are 9 analogue signal input channels in which digitisation is performed using ADCs with a maximum conversion rate of 400 MS/s, and 2 analogue output channels formed using DACs, which can be clocked at up to 210 MHz. The digital signal processing is based on a Xilinx Virtex5 FPGA [7]. The FPGA is clocked with a 357 MHz source derived from the ATF master oscillator and hence locked to the beam. The ADCs are clocked at 357 MHz. The analogue BPM processor output signals are sampled on peak to provide the input signals to the feedback. The gain stage is implemented via a lookup table stored in FPGA RAM, alongside the reciprocal of the sum signal for beam charge normalisation. The delay loop is implemented as an accumulator in the FPGA. The output is converted back to analogue and used as input to the driver amplifier. A pre-beam trigger signal is used to enable the amplifier drive output from the digital board.

The driver amplifier was manufactured by TMD Technologies [8] and provides ±30A of drive current into the kicker. The risetime is 35ns from the time of the input signal to reach 90% of peak output. The output pulse length was specified to be up to 10 microseconds.

BEAM TEST RESULTS

We report the results of beam tests of the system performed in 2011/12; earlier results were reported in [3,9]. We commissioned both the P2-K1 and P3-K2 loops (Figure 2). The latencies were measured to be 133ns (P2-K1) and 130ns (P3-K2). Each loop was first commissioned separately [3], and then in coupled-loop mode. For the purpose of obtaining optimal spatial correlations (see below) between the bunches in the extracted bunchtrain the ATF damping ring was set up so as to extract only two bunches, with a separation of 187.6ns. An example of a gain scan of the coupled system is shown in Figure 4, which shows the corrected position of the second bunch as measured in both P2 and P3.

On the basis of these studies the optimal gain for each loop was selected and the feedback was operated in coupled-loop mode. An example of the feedback performance is given in Figures 5 and 6, which show the RMS vertical beam position (the 'jitter') of bunch 2 measured at P2 and P3, respectively. With the feedback off the incoming jitter was measured to be 3.42um at P2 and 3.21um at P3. With the feedback on the measured jitter was 0.64um and 1.04um, respectively, representing correction factors of approximately 5 and 3 respectively.

The expected performance of the feedback can be calculated from the measured incoming jitter and knowledge of the bunch 1 – bunch 2 correlations. These correlations were measured to be 98% and 97% at P2 and P3, respectively. Using:

$$\sigma_2'^2 = \sigma_1^2 + \sigma_2^2 - 2\sigma_1\sigma_2\rho_{12} \geq 2\sigma_r^2$$

it follows that one expects corrected beam jitters of 0.64um and 0.83um for bunch 2 at P2 and P3 respectively, in very good agreement with the measured values. We conclude that the coupled-loop feedback is operating at close to the optimal performance given the degree of correlation between the two bunches.

ISBN 978-3-95450-115-1

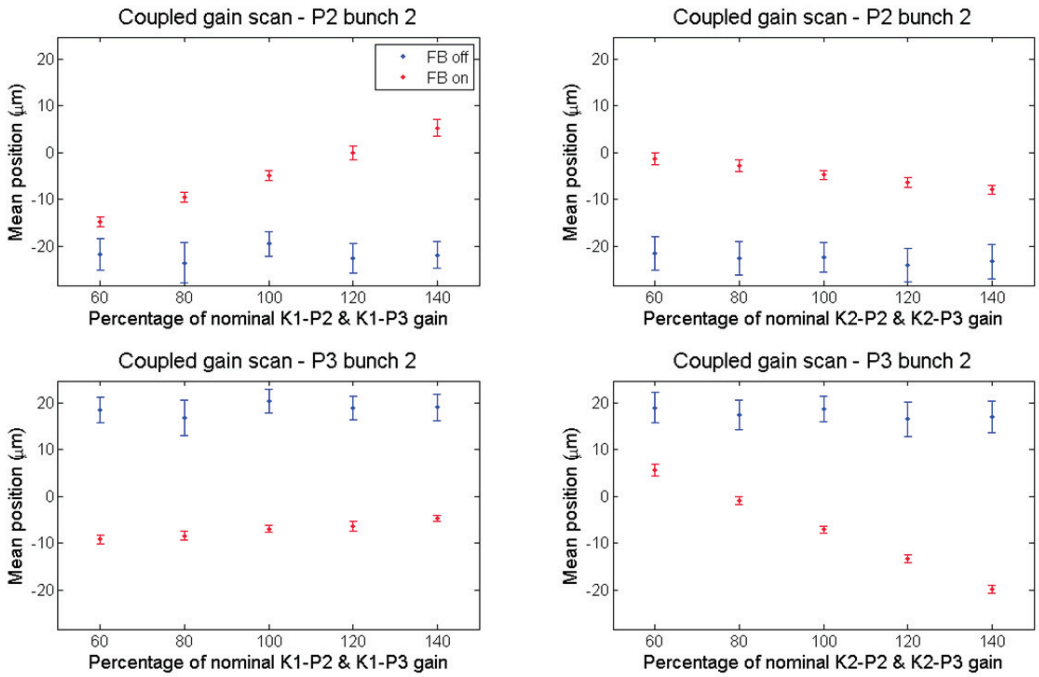

Figure 4: Vertical beam position for bunch 2 at P2 (top row) and at P3 (bottom row), versus feedback loop gain for K1 (left column) and K2 (Right column), without (blue) and with (red) feedback.

This measured performance of the system was input into a beam transport simulation [10] of the ATF2 beamline and the expected vertical beam position downstream of the FONT5 system was evaluated and compared with measurements. In the absence of additional jitter sources and lattice imperfections the performance is equivalent to stabilising the beam at the ATF2 IP to below the 10nm level [10].

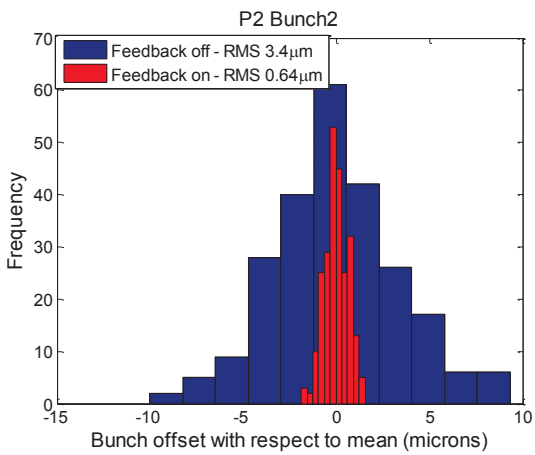

Figure 5: Distribution of vertical beam position for bunch 2 at P2, without (blue) and with (red) feedback.

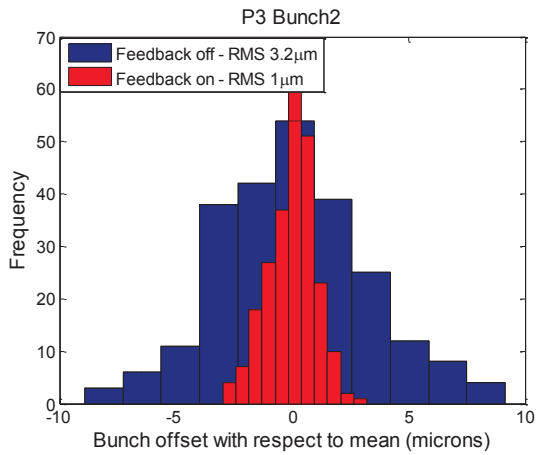

Figure 6: Distribution of vertical beam position for bunch 2 at P3, without (blue) and with (red) feedback.

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