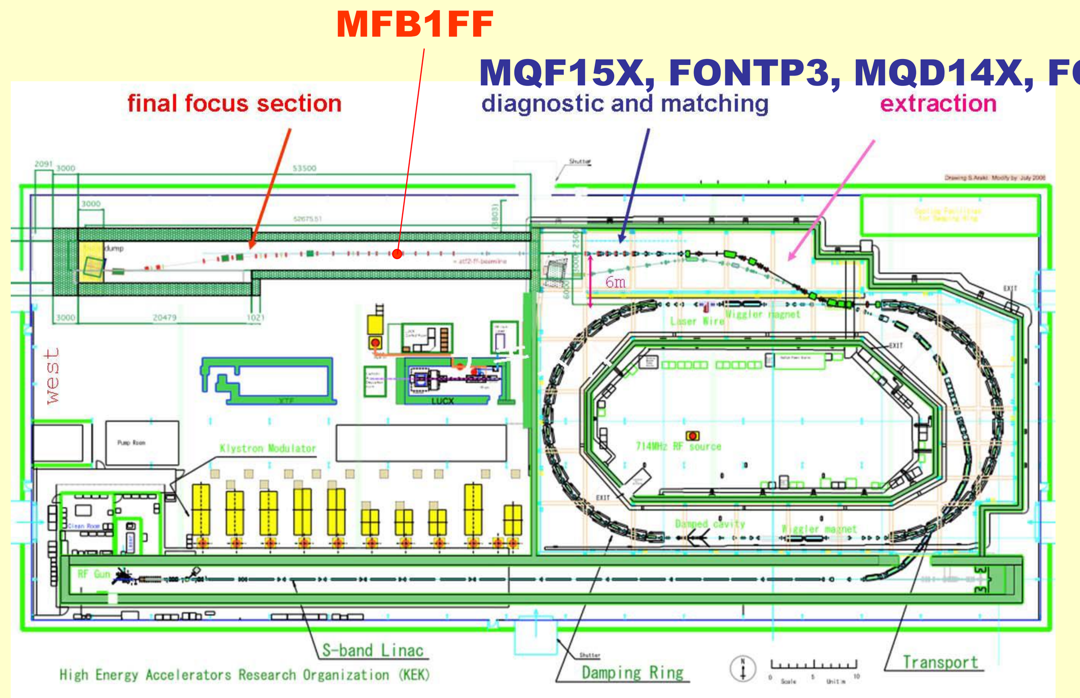
A low-latency sub-micron resolution stripline beam position monitoring system for single-pass beamlines

P.N. Burrows, D. R. Bett, N. Blaskovic Kraljevic, G.B. Christian, M. R. Davis, C. Perry, *John Adams Institute for Accelerator Science, Oxford, UK*
R. J. Apsimon, B. Constance, A. Gerbershagen, *CERN, Geneva, Switzerland*
J. Resta López, *IFIC, Valencia, Spain*

Abstract

A low-latency, sub-micron resolution stripline beam position monitoring system has been developed for use in single-pass beamlines. The fast analogue front-end signal processor is based on a single-stage RF down-mixer and is combined with an FPGA-based system for digitisation and further signal processing. The system has been deployed and tested with beam at the Accelerator Test Facility at KEK. Performance results are presented on the calibration, resolution and stability of the system. A detailed simulation has been developed that is able to account for the measured performance.

Stripline BPMs

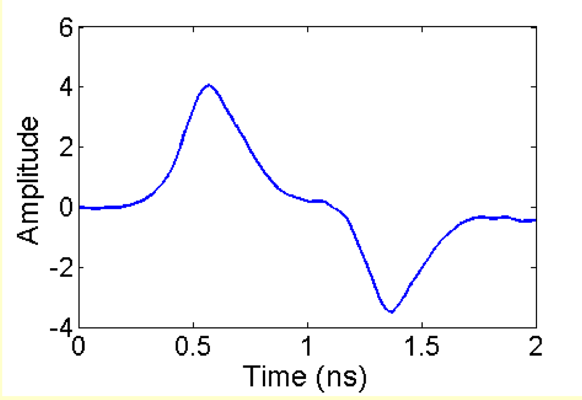


ATF, KEK, Japan

Stripline BPM FONTP1

Dimensions:

Length	120 mm
Radius	14 mm

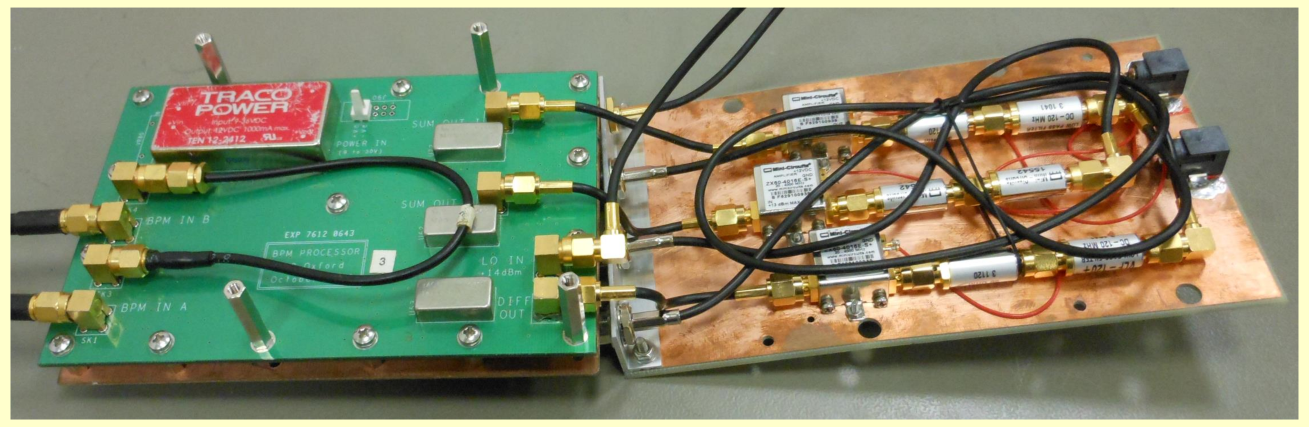


Stripline signal

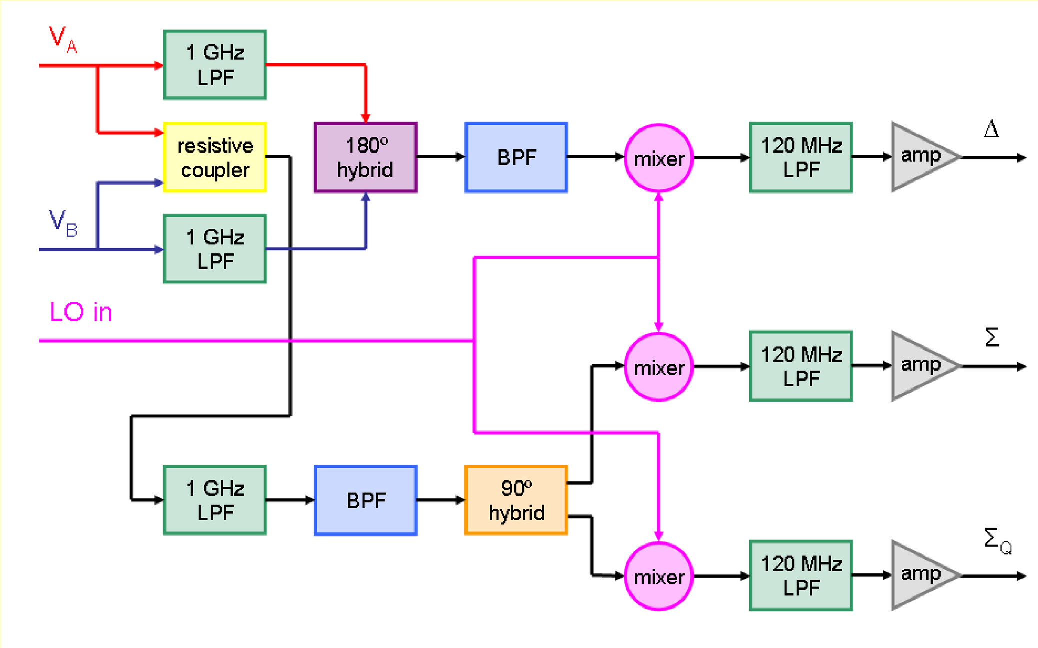
BPM Processor Design

Components:

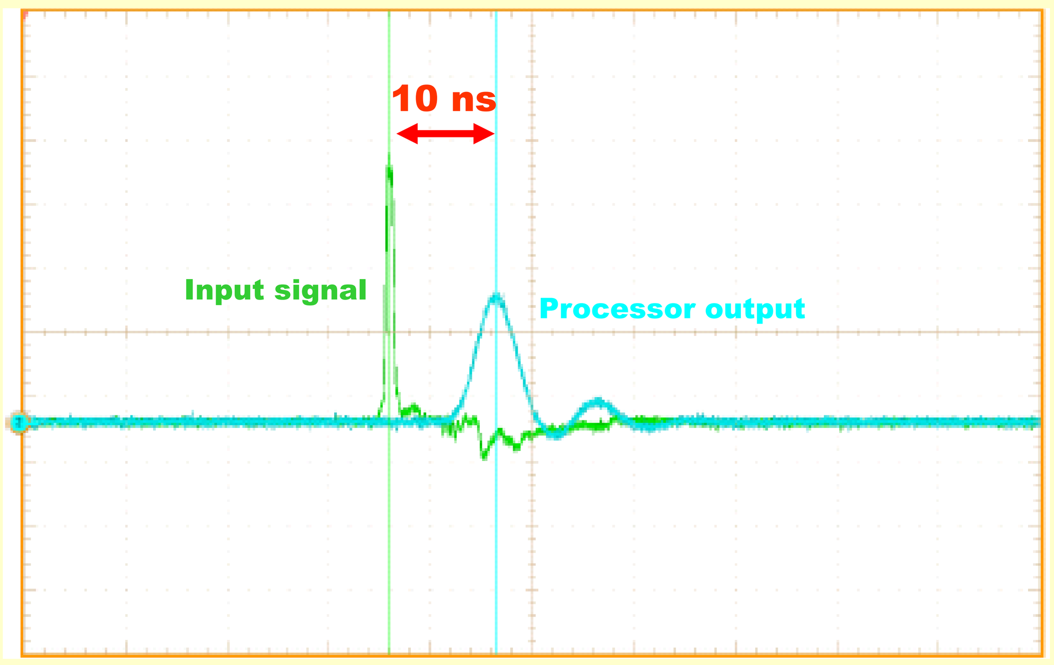
Resistive coupler	forms the raw sum of the input signals
180° hybrid	forms the difference of the input signals
90° hybrid	gives pair of sum signals 90° out of phase
Band-pass filters	reject unwanted frequencies
Mixers	down-mix to baseband using 714 MHz LO
Low-noise amps	boost signal levels by 16 dB



BPM processor module

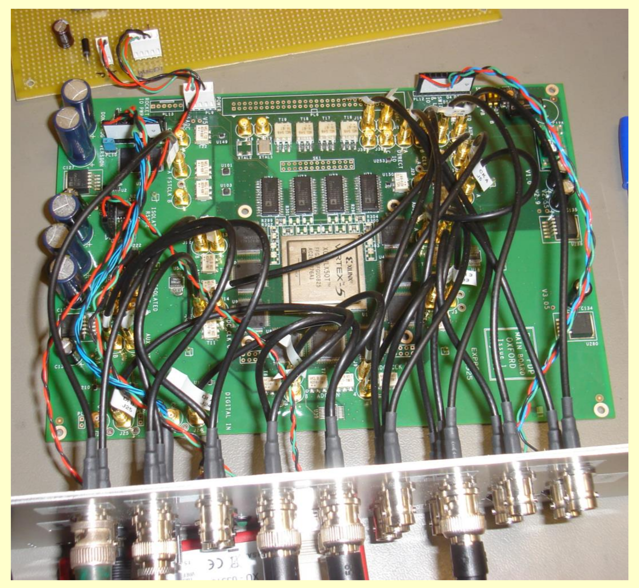


Schematic of BPM processor module



Scope trace from processor latency bench test

Digital Hardware



FONT5 digital board

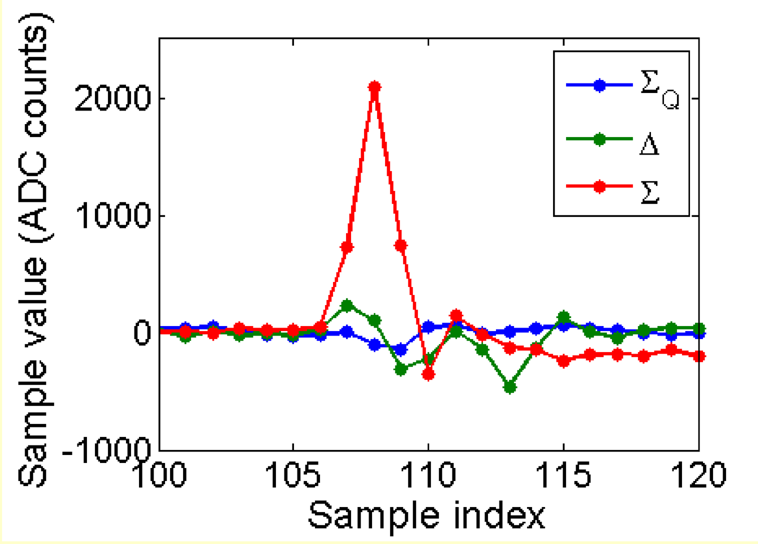
The FONT5 digital board is built around a Xilinx Virtex-5 FPGA. It features 9 14-bit ADCs clocked at 357 MHz; the sample clock has a variable delay in increments of 70 ps to facilitate sampling of the peak of the processor output signals. A serial interface is used for communication with the custom control software.

Presently 164 samples are returned per beam extraction.

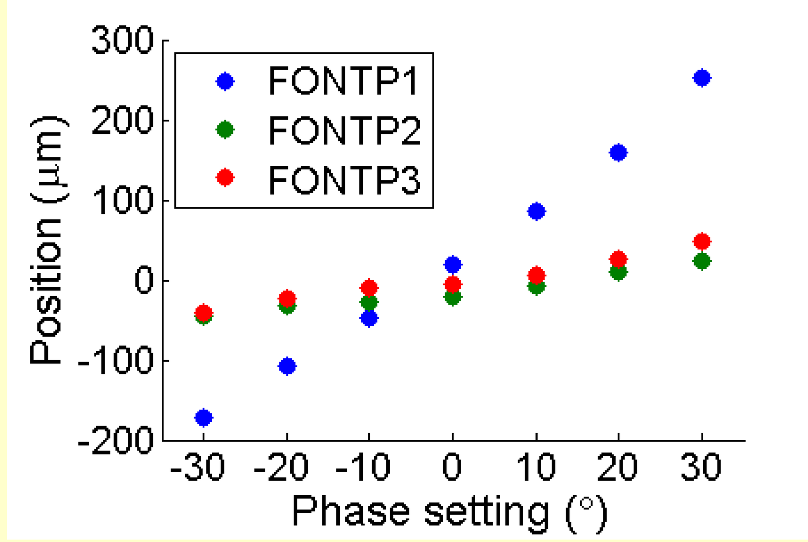
Position Determination

As part of the LO-based processing scheme, the LO input to each processor is phased so that the arrival of the bunch coincides with the peak amplitude of the LO. This condition is achieved when the sum is maximized; the sumQ is therefore very close to zero and is maximally sensitive to any phase offset between the LO and the bunch.

For stripline BPMs, the position of the bunch is proportional to the ratio of the difference to the sum. However, a change in the LO phase is observed to produce a spurious change in the measured position. The ratio of the sumQ to the sum is approximately equal to the phase offset in radians and is used to remove the contribution of the phase offset to position.



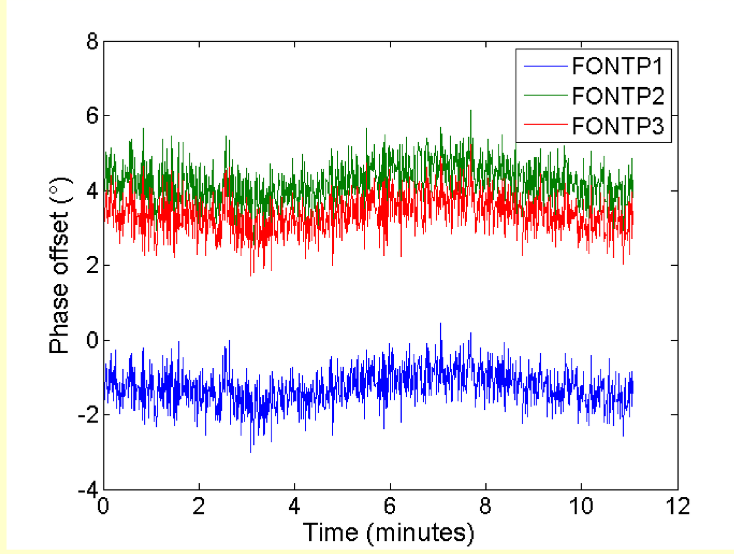
Digitized processor output signals



Effect of varying LO phase to processor

BPM	Phase sensitivity (microns per degree)
FONTP1	-7.0
FONTP2	-0.3
FONTP3	0.1
MQD14X	-1.6
MQF15X	0.6
MFB1FF	-1.0

Table of BPM response to LO phase offset. Parameters obtained by fitting position as a function of phase

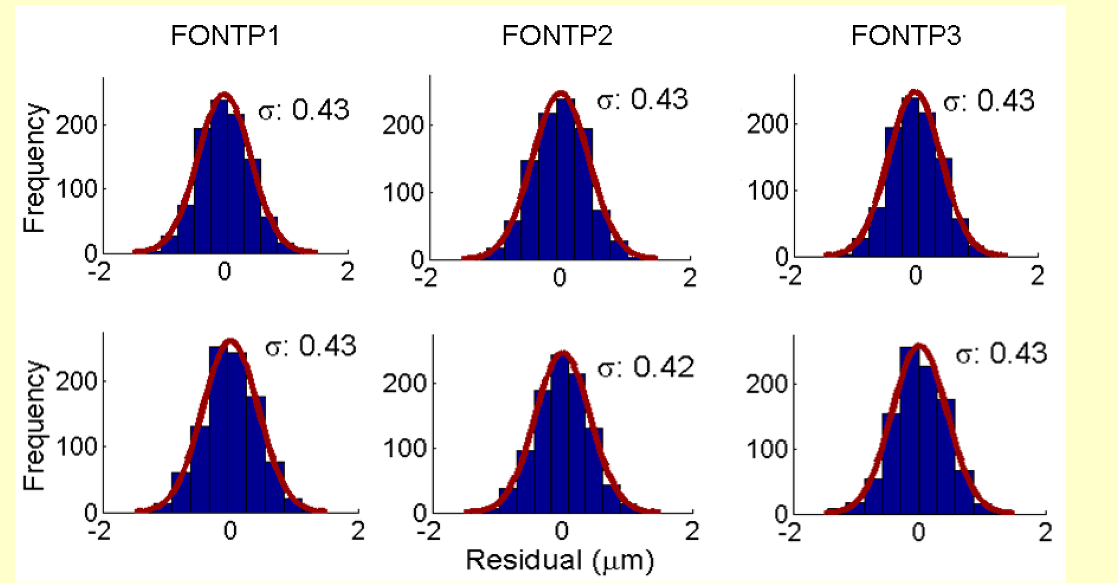


Natural variation of phase offset

By assuming that the position in a single BPM comprises a true position term and a term due to the phase offset at that BPM, the position can be fitted as a function of the phase offset to yield the sensitivity of that BPM to variations in LO phase

Resolution Determination

The three BPMs are assumed to have the same resolution. The positions in two of the BPMs are then used to predict the position in the third. The residual is the predicted position subtracted from the observed position; the resolution is the standard deviation of this (0.43 um).

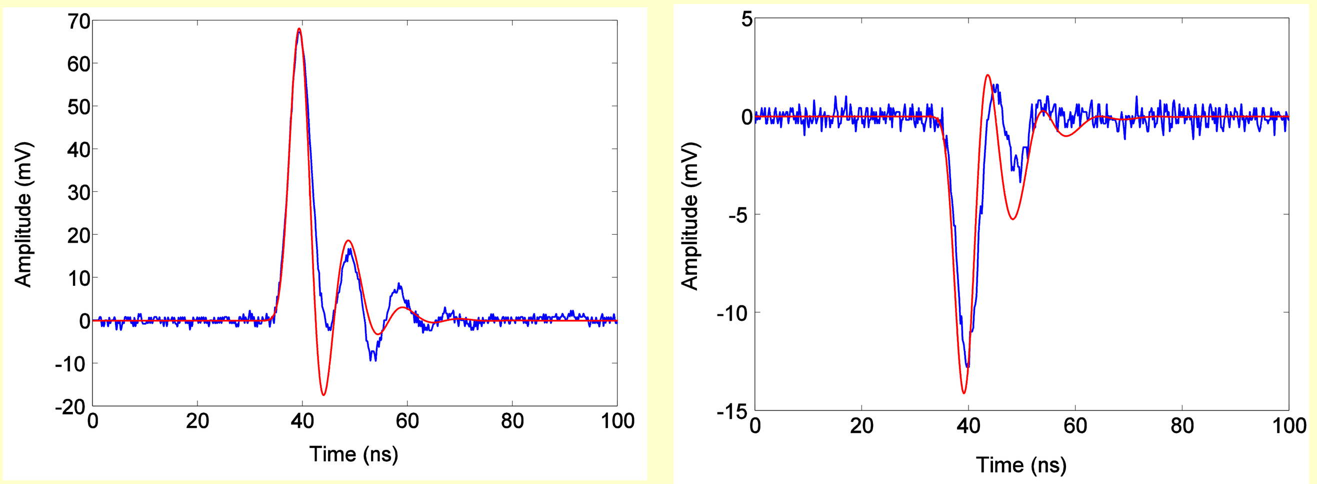


Residuals when the position in each BPM is predicted using the transfer matrices (top); from a least-squares fit to the position in the other BPMs (bottom)

Simulation

A complete simulation of the processor module was constructed by assembling simulations of the individual components. The analogue electronic circuit simulator SPICE was used to create models of the resistive coupler, mixer and filters; the 180° hybrid was simulated using MATLAB.

The model is able to accurately reproduce the key features of both the sum and difference signals.



Comparison between real (blue) and simulated (red) outputs of the sum (left) and difference (right) outputs of the processor module.

References

[1] http://www.linearcollider.org/cms/
[2] http://clic-study.web.cern.ch/CLIC-Study/
[3] www-pnp.physics.ox.ac.uk/~font/
[4] D. Bett et al, these proceedings, WEPPP068
[5] http://www-atf.kek.jp.atf/
[6] R. J. Apsimon, DPhil thesis, University of Oxford
[7] B. Constance, DPhil thesis, University of Oxford