Latest Performance Results from the FONT5 Intra-train Position and Angle Feedback System at ATF2

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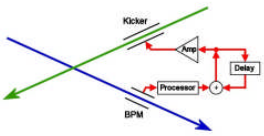
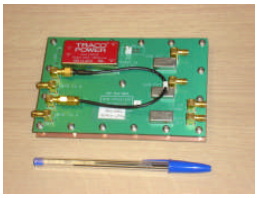
Abstract

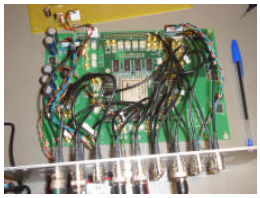
A prototype Interaction Point beam-based feedback system for future electron-positron colliders, such as the International Linear Collider, has been designed and tested on the extraction line of the KEK Accelerator Test Facility (ATF). The FONT5 intra-train feedback system aims to stabilise the beam orbit by correcting both the position and angle jitter in the vertical plane on bunch-to-bunch timescales, providing micron-level stability at the entrance to the ATF2 final-focus system. The system comprises three stripline beam position monitors (BPMs) and two stripline kickers, custom low-latency analogue front-end BPM processors, a custom FPGA-based digital processing board with fast ADCs, and custom kicker-drive amplifiers. An overview of the hardware, and the latest results from beam tests at ATF2, will be presented. A total system latency as low as approximately 140 ns has been demonstrated.



Linear Collider Interaction Point feedback concept

- **Measure beam-beam deflection angle of outgoing beam with Beam Position Monitor (BPM), and hence offset at IP**
- **Correct other beam, incoming to IP using fast amplifier and kicker**
- **Prototype digital position and angle system developed and tested at ATF, KEK**





Hardware & System Design

FPGA-based digital feedback processor

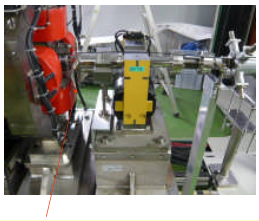
- **Xilinx Virtex5 FPGA**
- **9 analogue input channel and two DAC outputs**
- **FPGA and ADCs clocked at 357 MHz, synchronised to ATF**

Analogue Front-End Processor:

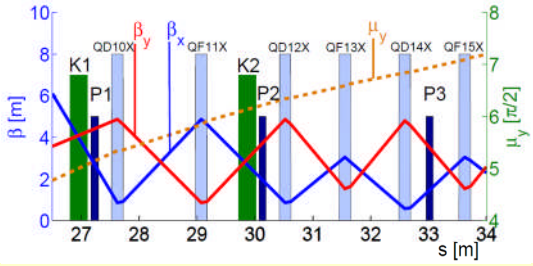
- **Down-mixes raw stripline signals to baseband**
- **Forms sum and difference signal from opposing strips**
- **Latency ~10 ns**

TMD Kicker Drive Amplifier

Kicker K1 on ATF beamline



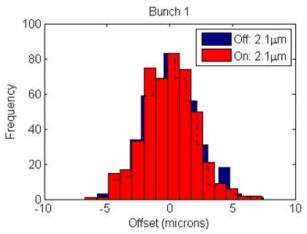
BPM P1 on ATF beamline

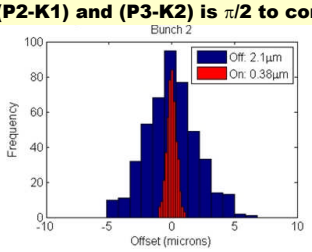


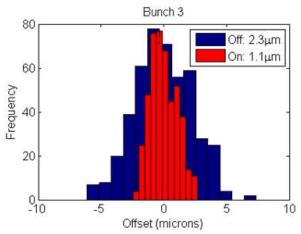
Layout of FONT5 bunch-by-bunch two-phase feedback system at ATF, showing the relative locations of the BPMs (P1,P2,P3) and the kickers (K1,K2). The nominal phase advance between the two loops (P2-K1) and (P3-K2) is $\pi/2$ to correct both position and angle.

System Specifications

System Resolution (BPM processor)	**<1 μm**
System Latency	**<150 ns**
Amplifier/ Kicker Bandwidth	**~30 MHz**
Dynamic Range of feedback system	**+/- ~100 μm (>46 dB)**
Dynamic range of the BPM system	**+/- ~500 μm (>60 dB)**

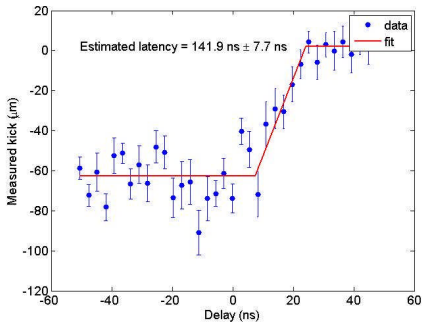




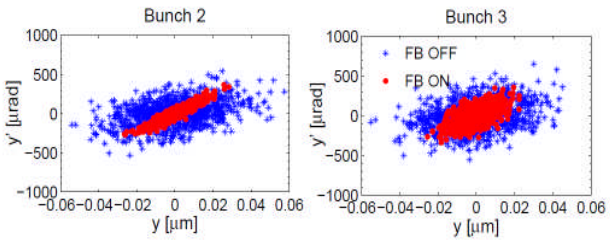


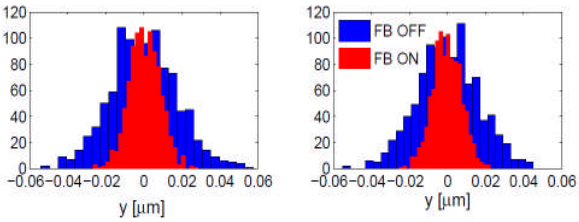
Position distributions for the three bunches at P2 showing the reduction in measured beam jitter with coupled feedback operation, with interleaved feedback off (blue) and feedback on (red). A rolling average is subtracted from each bunch position to remove the effects of position drift from the jitter distributions. The corrections observed for each bunch were as would be expected given the measured incoming jitter and bunch-to-bunch correlations observed.

Recent Results



Latency estimate for the P3-K1 feedback loop. Average difference between kicked and un-kicked positions for bunch 2 at P3, as a function of additional delay applied to the constant amplifier drive.





Predicted position and angle correlation (top) and position distributions (bottom) for bunch 2 (left) and bunch 3 (right) at the ATF2 virtual IP, with feedback off (blue) and feedback on (red), simulated using the nominal model for the final focus, and the measured position jitters at the feedback BPMs, P2 and P3. The simulation assumes no extra source of jitter downstream of the feedback system. See reference [9] for more information.

References

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[2] http://clic-study.web.cern.ch/CLIC-Study/
[3] P.N. Burrows et al, Proceedings PAC03, Portland, Oregon, May 2003, p. 687.
[4] P.N. Burrows et al, Proceedings EPAC04, Lucerne, July 2004, p. 785.
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