Latest beam test results from ATF2 with the FONT ILC prototype intra-train beam feedback systems

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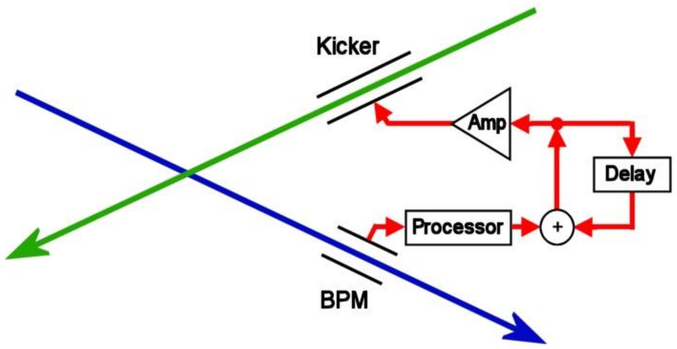
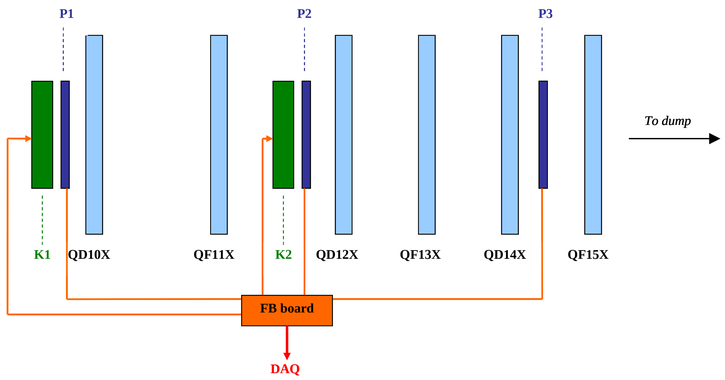
Linear Collider intra-train IP feedback concept:



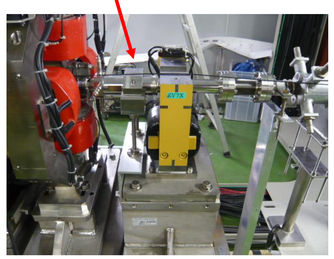
Detect position offset of incoming bunches early in train. Calculate correction and apply with kicker to later bunches

FONT5 digital prototype at KEK ATF2:

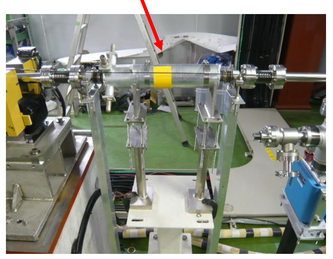


ATF2 extraction line:

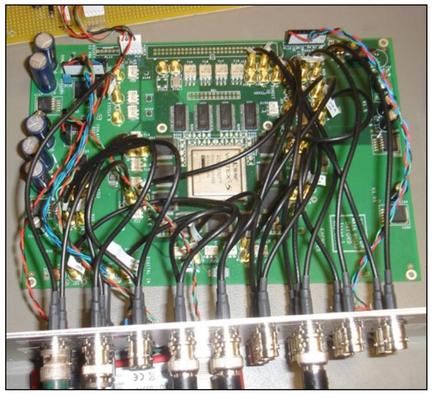
BPM P1



Kicker K1



Digital feedback processor:



Xilinx Virtex5 FPGA

Clocked at 357 MHz phase-locked to beam

4x faster than FONT4

9 ADC input channels (TI ADS5474)

4 DAC output channels (AD9744)

Latency estimate:

- Time of flight kicker – BPM: 12ns
- Signal return time BPM – kicker: 32ns

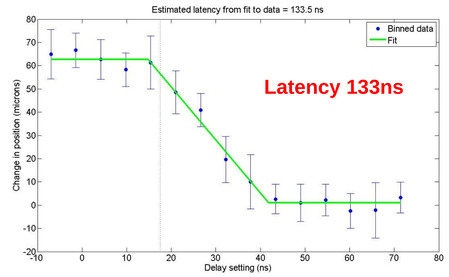
  Irreducible latency: 44ns

- BPM processor: 10ns
- ADC/DAC (4.5 357 MHz cycles) 14ns
- Signal processing (8 357 MHz cycles) 22ns
- FPGA i/o 3ns
- Amplifier 35ns
- Kicker fill time 3ns

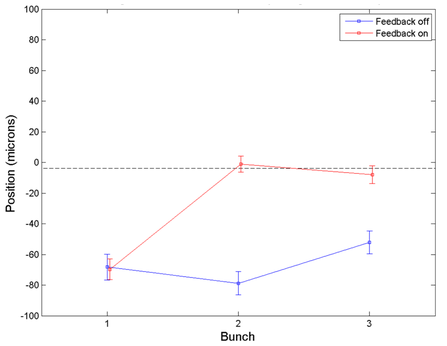
  Electronics latency: 87ns

- Total latency budget: 131ns

Beam test results:

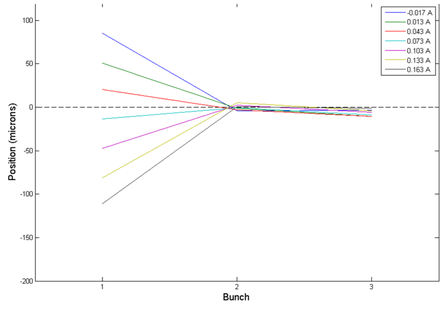


Direct latency measurement via kicker timing scan



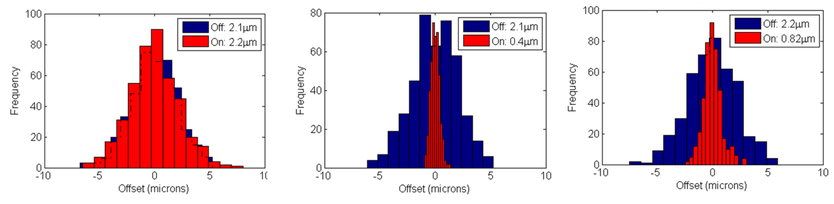
Example incoming bunchtrain:

Action of main loop, delay loop, and 'banana' correction



Scan over incoming bunchtrain positions

Feedback correction of incoming bunchtrain jitter



Jitter reduced by factor of 5