Design and performance of a prototype digital feedback system for the ILC

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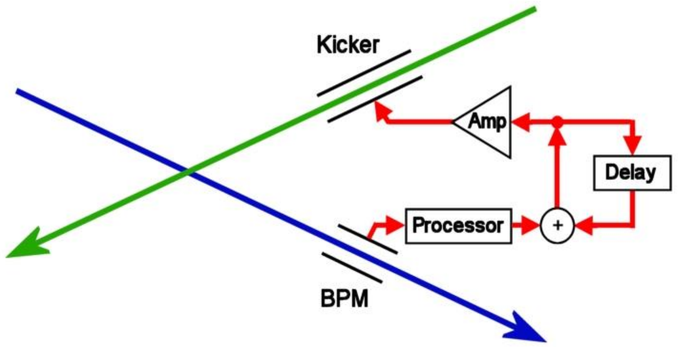
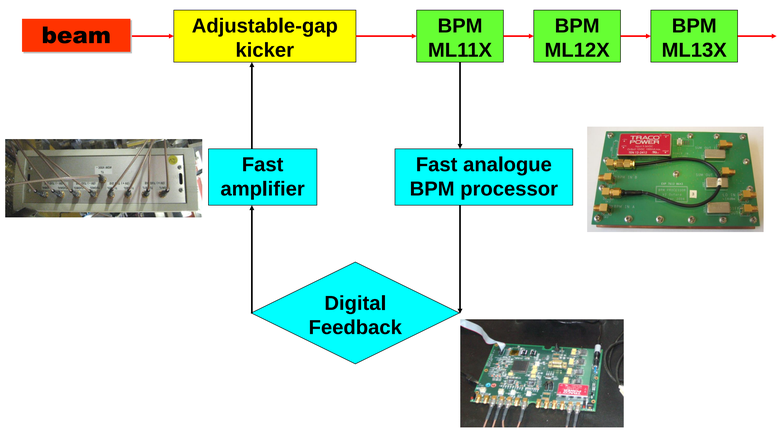
Linear Collider intra-train IP feedback concept:

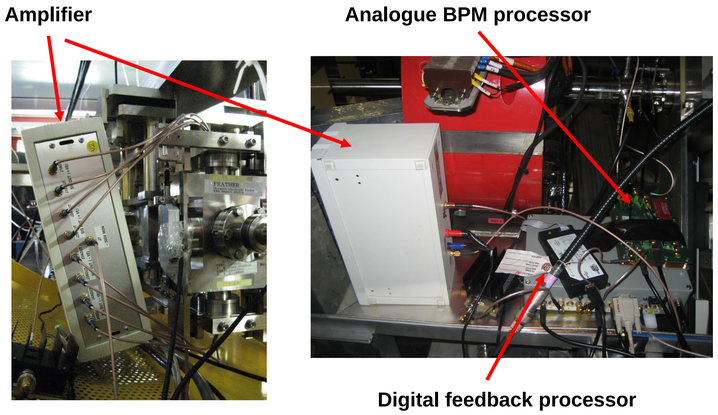


Detect position offset of incoming bunches early in train. Calculate correction and apply with kicker to later bunches

FONT4 digital prototype at KEK ATF:



ATF extraction line:

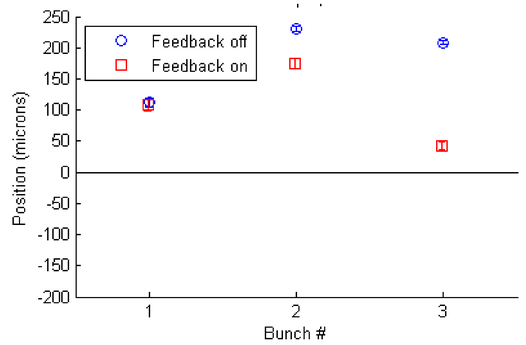


Digital feedback processor:

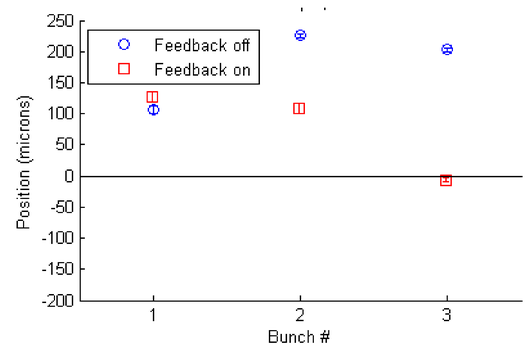
Latency estimate:

• Time of flight kicker – BPM:	4ns
• Signal return time BPM – kicker:	10ns
Irreducible latency:	14ns
• BPM processor:	10ns
• ADC/DAC (3.5 89 MHz cycles)	40ns
• Signal processing (9 357 MHz cycles)	27ns
• FPGA i/o	3ns
• Amplifier	35ns
• Kicker fill time	3ns
Electronics latency:	118ns
• Total latency budget:	132ns

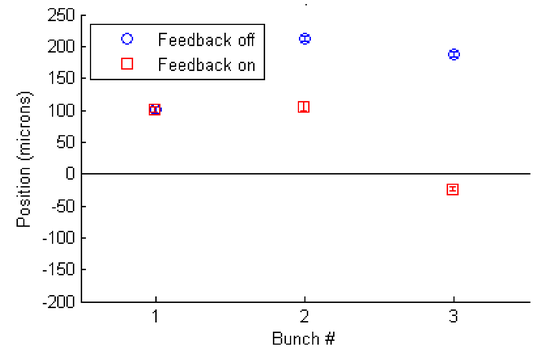
Beam test results:



Low gain

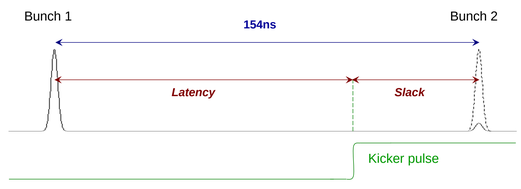


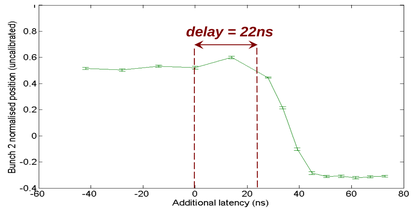
'Optimal' gain



High gain

Latency measurement:





Latency = 154 – 22 = 132ns + 8ns (charge normalisation) = 140ns total