DESIGN AND PERFORMANCE OF A PROTOTYPE DIGITAL FEEDBACK SYSTEM FOR THE INTERNATIONAL LINEAR COLLIDER INTERACTION POINT

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Abstract

We present the design and preliminary results of a prototype beam-based digital feedback system for the Interaction Point of the International Linear Collider. A custom analogue front-end processor, FPGA-based digital signal processing board, and kicker drive amplifier have been designed, built, and tested on the extraction line of the KEK Accelerator Test Facility (ATF). The system was measured to have a latency of approximately 140 ns.

INTRODUCTION

A number of fast beam-based feedback systems are required at the International electron-positron Linear Collider (ILC) [1]. At the interaction point (IP) a very fast system, operating on nanosecond timescales within each bunchtrain, is required to compensate for residual vibration-induced jitter on the final-focus magnets by steering the electron and positron beams into collision. A pulse-to-pulse feedback system is envisaged for optimising the luminosity on timescales corresponding to 5 Hz. Slower feedbacks, operating in the 0.1 – 1 Hz range, will control the beam orbit through the Linacs and Beam Delivery System.
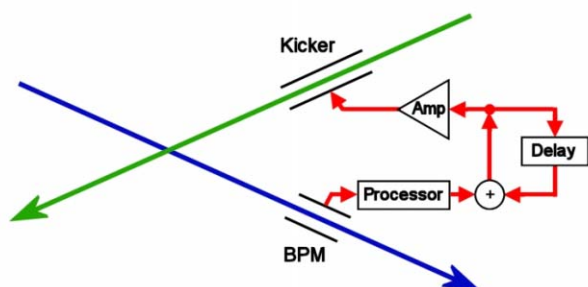

Figure 1: Schematic of IP intra-train feedback system with a crossing angle. The deflection of the outgoing beam is registered in a BPM and a correcting kick applied to the incoming other beam.

The key components of each such system are beam position monitors (BPMs) for registering the beam orbit; fast signal processors to translate the raw BPM pickoff signals into a position output; feedback circuits, including delay loops, for applying gain and taking account of system latency; amplifiers to provide the required output drive signals; and kickers for applying the position (or angle) correction to the beam. A schematic of the IP intra-train feedback is shown in Figure 1, for the case in which

the beams cross with a small angle; the current ILC design incorporates a crossing angle of 14 mrad.

Critical issues for the intra-train feedback performance include the latency of the system, as this affects the number of corrections that can be made within the duration of the bunchtrain, and the feedback algorithm. Previously we have reported on all-analogue feedback system prototypes in which our aim was to reduce the latency to a few tens of nanoseconds, thereby demonstrating applicability for 'room temperature' Linear Collider designs with very short bunchtrains of order 100ns in length, such as NLC, GLC and CLIC [2]. We achieved total latencies (signal propagation delay + electronics latency) of 67ns (FONT1) [3], 54ns (FONT2) [4] and 23ns (FONT3) [5].

We report the latest results on the design, development and beam testing of an ILC prototype system that incorporates a digital feedback processor based on a state-of-the-art Field Programmable Gate Array (FPGA) [6]. The use of a digital processor will allow for the implementation of more sophisticated algorithms which can be optimised for possible beam jitter scenarios at ILC. However, a penalty is paid in terms of a longer signal processing latency due to the time taken for digitisation and digital logic operations. This approach is now possible for ILC given the long, multi-bunch train, which includes parameter sets with c. 3000/6000 bunches separated by c. 300/150ns respectively. Initial results were reported previously [7,8].

FONT4 DESIGN

A schematic of the FONT4 feedback system prototype and the experimental configuration in the ATF extraction beamline is shown in Figure 2. The layout is functionally equivalent to the ILC intra-train feedback system. An upstream dipole corrector magnet can be used to steer the beam so as to introduce a controllable vertical position offset in stripline BPM ML11X. The BPM signal is initially processed in a front-end analogue signal processor. The analogue output is then sampled, digitised and processed in the digital feedback board to provide an analogue output correction signal. This signal is input to a fast amplifier that drives an adjustable-gap stripline kicker [9], which is used to steer the beam back into nominal vertical position. BPMs ML12X and ML13X can serve as independent witnesses of the beam position.
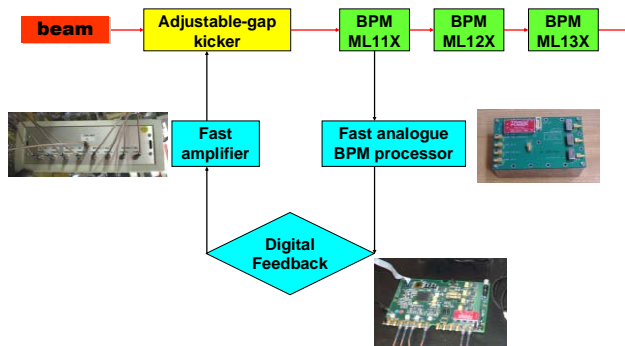
Figure 2: Schematic of FONT4 at the ATF extraction beamline showing the relative locations of the kicker, BPMs and the elements of the feedback system.

The ATF damping ring can be operated so as to provide an extracted train that comprises 3 bunches separated by an interval that is tuneable in the range 140 - 154 ns. This provides a short ILC-like train which can be used for controlled feedback, or feed-forward [10] system tests.

FONT4 has been designed [7] as a bunch-by-bunch feedback with a latency goal of less than 140ns. This meets the minimum ILC specification of c. 150ns bunch spacing, as well as the smallest spacing allowed at ATF. This will allow measurement of the first bunch position and correction of both the second and third ATF bunches. The correction to the third bunch is important as it allows test of the 'delay loop' component of the feedback, which is critical for maintaining the appropriate correction over a long ILC bunchtrain.

The design of the front-end BPM signal processor [7] is based on that for FONT3 [5]. The top and bottom (y) stripline BPM signals were added and subtracted using a hybrid, to form a sum and difference signal respectively. The resulting signals were band-pass filtered and down-mixed with a 714 MHz local oscillator signal which was phase-locked to the beam. The resulting baseband signals are low-pass filtered. The hybrid, filters and mixer were selected to have latencies of the order of a few nanoseconds, in an attempt to yield a total processor latency in the range 5-10ns. The output pulse is illustrated in Figure 3. The measured latency is around 10ns [7,8].

The custom digital feedback processor board is shown in Figure 4. There are two analogue signal input (output) channels in which digitisation is performed using Analog Devices ADCs (DACs) which can be clocked at up to 105 (210) Ms/s. The digital signal processing is based on a Xilinx Virtex4 FPGA [6] which can be clocked at up to 500MHz. The FPGA is clocked with a 357 MHz source, derived from the ATF master oscillator and hence locked to the beam. Logic operations are triggered with a pre-beam signal. The ADC/DAC are clocked at 357/4 Ms/s. The analogue BPM processor output signal is sampled at the peak to provide the input signal to the feedback.
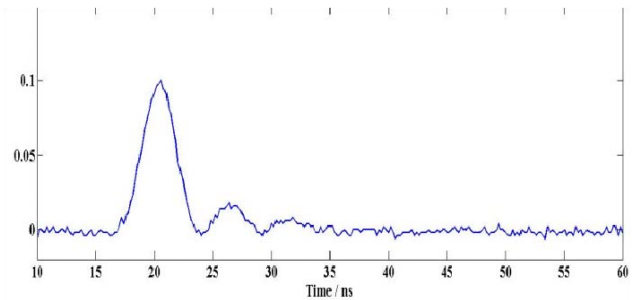

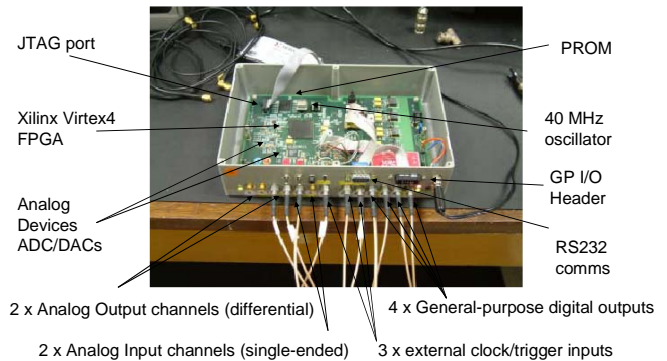Figure 3: Voltage output of BPM signal processor.

Figure 4: FONT4 digital feedback board.

The gain stage is implemented via a lookup table stored in FPGA RAM, alongside the reciprocal of the sum signal for charge normalisation. The delay loop is implemented as an accumulator on the FPGA. The output is converted back to analogue and used as input to the driver amplifier.

The driver amplifier was manufactured by TMD Technologies [11], a UK-based RF company. The amplifier was specified to provide +-30A of drive current into the kicker [8], whose striplines were shorted at the upstream end (nearer the incoming beam). The risetime, starting at the time of the input signal, was specified as 35ns to reach 90% of peak output. The output pulse length was specified to be up to 10 microseconds. Although current operation is with only 3 bunches in a train of length c. 300ns, it is planned in future to operate ATF with extracted trains of 20 or 60 bunches with similar bunch spacing; the design allows for this upgrade.

BEAM TEST RESULTS

We report the preliminary results of the most recent beam tests, performed in May 2008. The beam was steered successively into different vertical positions spanning a range of about +-200 microns centred around nominal zero. An example is shown in Figure 5. The data shown are the averages over 10 or 11 pulses. The feedback is seen to under- and over-correct for low and high gain, respectively, and it is possible to make a 'perfect' correction of bunch 3 by an appropriate gain choice. It should be noted, however, that the bunchtrain is not straight, there being a sagitta of order 100 microns between the incoming bunches, and this complicates the

operation of the feedback system. Nevertheless the system works as expected.
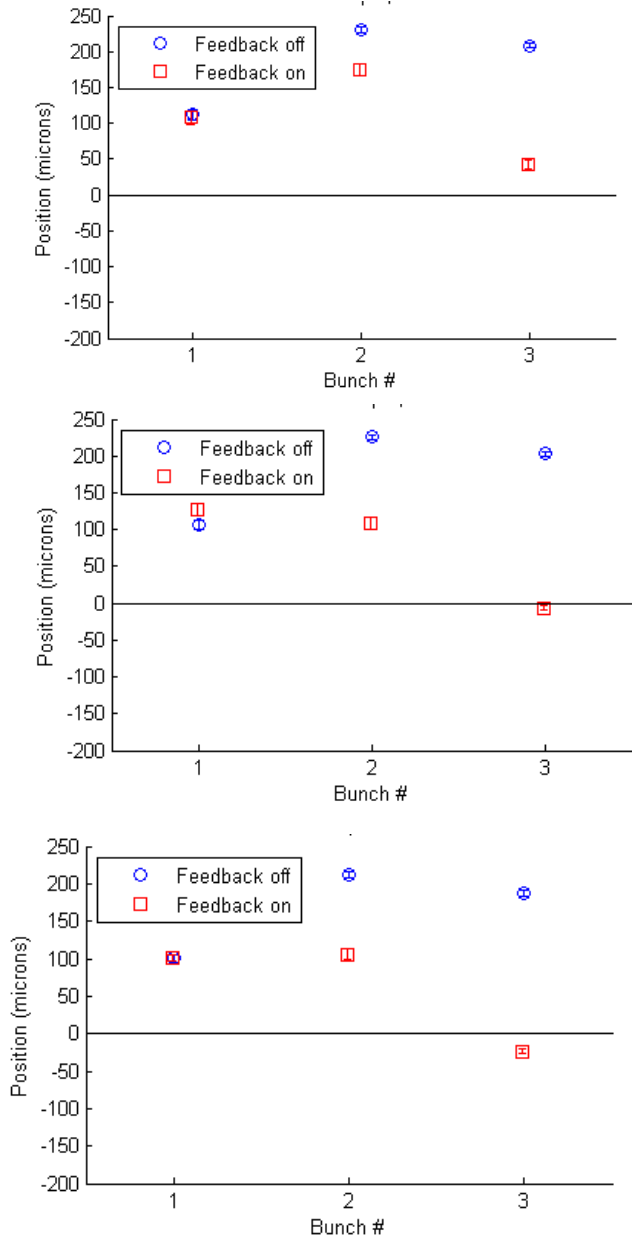

Figure 5: Beam position vs. bunch number: low (top), medium (middle) and high (bottom) gain.

The latency was measured by deliberately delaying the kick to bunch 2, and observing the kick vs. added delay (Figure 6). This used a special version of the FPGA firmware, without the inclusion of real-time charge normalisation. The delay at which bunch 2 stops being kicked, defined as 90% of full kick to bunch 2, corresponds to a latency equal to the bunch spacing. The difference between the 90% kick point and zero added delay gives a measure of the amount of timing slack in the system, and hence, subtracting this from the bunch spacing of 154 ns yields a latency of c. 132 ns. The constituents of the system latency are shown in Table 1. The inclusion of real-time charge-normalisation uses an
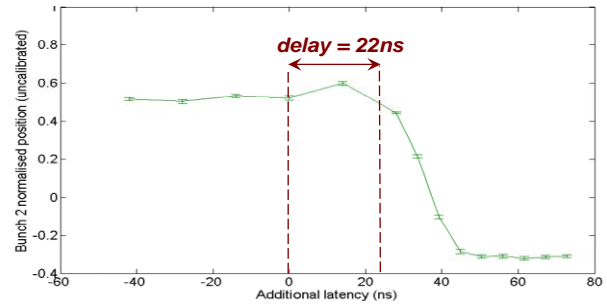
extra 3 clock cycles in the FPGA firmware, increasing the system latency by 8.4ns to c.140ns.

Figure 6: Kick to bunch 2 vs. added delay.

Table 1: Latency constituents for the FONT4 system.

Source of delay	Contribution to latency (ns)
Beam time-of-flight	4
Signal return time	10
BPM processor	10
Digital processor	77
Amplifier risetime	35
Kicker fill time	3
Total	**139**

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