Linear Collider intra-train feedback concept:

Detect position offset of incoming bunches early in train. Calculate correction and apply with kicker to later bunches.

**ATF extraction line:**

- Analogue BPM processor
- Amplifier/FB board

**Analogue BPM signal processor:**

- Stripline BPM inputs
- Amplifier
- Mixer
- Processor output

**Digital feedback processor design:**

- Xilinx Virtex4 FPGA

**Latency budget:**

- Time of flight kicker – BPM: 7ns
- Signal return time BPM – kicker: 15ns
- Irreducible latency: 22ns
- BPM processor: 7ns
- ADC/DAC: 40ns
- FPGA processing: 3ns
- I/O: 3ns
- Amplifier: 40ns
- Kicker fill time: 3ns
- Electronics latency: 118ns
- Total latency budget: 140ns

**Beam test results:**

- Analogue input from BPM processor
- Digital processor output