



^{{1]} John Adams Institute, Oxford University, UK

^[2] *IFIC, Valencia, Spain*

Linear Collider intra-train IP feedback concept:



Detect position offset of incoming bunches early in train. Calculate correction and apply with kicker to later bunches



BPM P1



Kicker K1



An FPGA-based Bunch-by-Bunch Position and Angle Feedback System at ATF2

Digital feedback processor:



Beam test results: single loop: K1 to P2









Single loop feedback can only correct the beam jitter at one point in the extraction line





maintained over an extended distance

Xilinx Virtex5 FPGA

Clocked at 357 MHz phase-locked to beam

9 ADC input channels (TI ADS5474)

4 DAC output channels (AD9744)

between bunches



Offset (microns)



Measurement of the latency of the K1 to P3 feedback loop. This is the longest feedback path in the FONT system and is therefore the critical path. The latency must be less than 154ns for bunch to bunch feedback to be achieved.



Feedback latency measurements: