

AN FPGA-BASED TURN-BY-TURN BEAM POSITION MONITORING SYSTEM FOR STUDYING MULTIPLE BUNCH BEAMS IN THE ATF DAMPING RING

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Abstract

Instabilities associated with beam-size blow-up have previously been observed with multi-bunch beam in the damping ring (DR) of the KEK Accelerator Test Facility (ATF). A system has been developed to monitor such instabilities, utilising an ATF stripline beam position monitor (BPM) in the DR, and BPM processor hardware designed for the FONT upstream feedback system in the ATF extraction line. The system is designed to record the horizontal and/or vertical positions of up to three bunches in the DR in single-bunch multi-train mode or the head bunch of up to three trains in multi-bunch mode, with a bunch spacing of 5.6 ns. The FPGA firmware and data acquisition software were modified to record turn-by-turn data for up to six channels and 1–3 bunches in the DR. The maximum memory configuration on the FPGA allows 131071 bunch-turn-channels of data to be recorded from a particular machine phase, and the system has the capability to select only certain turns at a regular interval in which to record data, in order to zoom out and cover the entire period of the damping cycle at the ATF. An overview of the system and initial results will be presented.

INTRODUCTION

The next generation of high energy linear lepton colliders, such as the International Linear Collider (ILC) [1] and the Compact Linear Collider [2], will require ultra-stable low-emittance multi-bunch beams to be preserved up to the Interaction Point. The KEK Accelerator Test Facility (ATF) [3] was originally constructed to demonstrate the generation of ultra-low emittance beams in the Damping Ring (DR). The ATF consists of a 1.2 GeV S-band linac, a 138 m circumference damping ring, and extraction line. Up to three trains can be injected into the DR during one machine cycle, with up to ten bunches per train at 5.6 ns bunch spacing.

Instabilities associated with beam-size blow-up have previously been observed on occasion with an X-ray Synchrotron Radiation (XSR) monitor, located in the ATF DR, when three or more bunches have been present in the DR. These periods of instability were correlated with approximately an order of magnitude larger beam

jitter and almost complete lack of bunch-to-bunch correlation in the extraction line. The underlying cause of these instabilities has so far not been understood, and the DR turn-by-turn button-style beam position monitors (BPMs) are not capable of bunch-by-bunch measurement within a single turn. To address this need a monitoring system has been developed using an available strip-line BPM in the DR, and BPM processing and digitisation hardware originally designed for the upstream feedback system in the extraction line[2]. The system has the ability to monitor up to three bunches in the DR on a turn-by-turn basis in multi-train single-bunch mode, or the leading bunch of each train in multi-bunch mode.

SYSTEM DESIGN

Hardware

The hardware for the turn-by-turn (TBT) system consists of a strip-line BPM in the ATF DR (sets of pick-ups in the horizontal and vertical plane are used), and a front-end analogue BPM processor and FPGA-based digital signal processor, both of which were designed for use in the FONT upstream feedback system in the ATF extraction line [4].

One analogue front-end is used for each transverse plane; the function being to convert the high frequency strip-line impulse signals to baseband (<100 MHz). An RF hybrid is used to form a sum and difference signal from the two opposing strips, which is then band-pass filtered and mixed with a 714 MHz local oscillator phase-locked to the beam, and finally low-pass filtered to remove the high frequency component of the mixer output.

The digital processor centres around a Xilinx Virtex-5 FPGA, clocked with both an external source of 357 MHz, synchronised to the ATF master oscillator for high speed logic including timing and synchronisation, and a 40 MHz from an on-board crystal oscillator for slower ancillary logic. High speed Analog Devices ADCs, also clocked at 357 MHz, digitise up to 9 channels of sum and difference signals from the front-end processors. The board is controlled, and data is transmitted, via a UART over RS-232.

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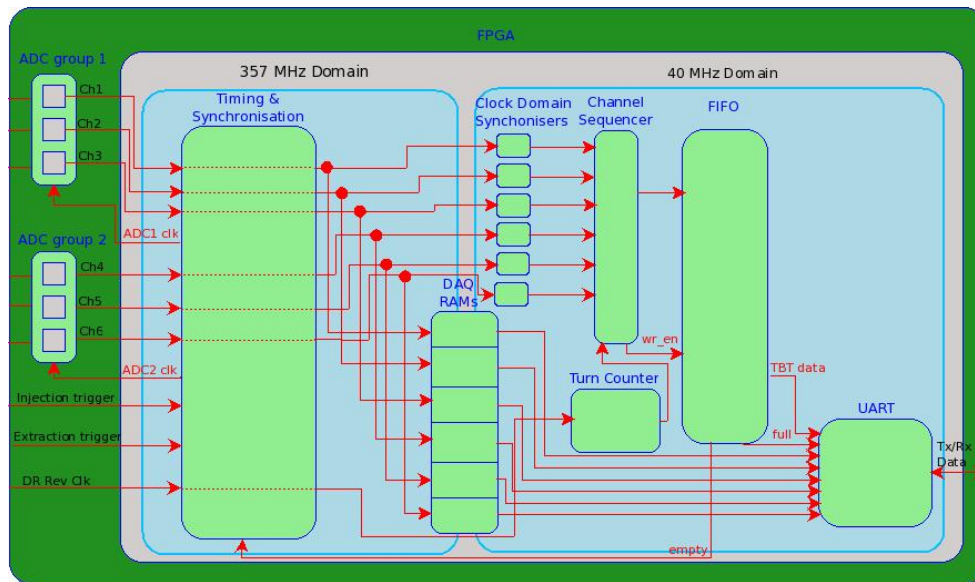


Figure 1: Simplified block diagram of the turn-by-turn firmware.

Firmware and Data Acquisition

The FPGA firmware and DAQ software were based on that developed for the FONT5 feedback system experiment in the ATF extraction line [4]. The main modifications to the firmware were to maximise the use of the available on-chip dedicated memory blocks, increase the UART speed and remove firmware blocks specific to the feedback. In the feedback firmware only 164 samples per channel per pulse (corresponding to one entire damping ring period sampled at 357 MHz). For DAQ from 9 channels, this requires only a maximum of 8% of the available Block RAM (BRAM) resources. To maximise the number of turns recorded for turn-by-turn (TBT) acquisition, it was decided to record only the peak value for each bunch and reduce the maximum number of channels recorded to six (allowing for horizontal and vertical position from a maximum of two BPMs in the DR). It was desirable to also retain the capability of returning all samples from one entire single-turn as for the feedback firmware, thereby allowing the user to determine the samples in each DR period corresponding to the bunches. This single turn is taken to be the last-turn before extraction from the DR, but this is arbitrary.

A block diagram of the turn-by-turn firmware is shown in Fig. 1. The incoming data streams from the six channels are multiplexed into a channel sequencer which selects which samples from which channels are to be recorded, and passes the relevant samples into a single large first-in, first-out (FIFO) memory. This FIFO comprises 112 x 18 kb cascaded BRAMs (93% of total resource), allowing a total of 131071 14-bit samples to be recorded per pulse, the remaining BRAM reserved for single-turn DAQ.

The system uses two triggers: an extraction trigger to select the last turn for single-turn acquisition; and an injection trigger to prompt the start of the TBT acquisition logic. The FPGA logic is clocked on two distinct domains: a fast domain, using an external 357 MHz

source synchronised to the beam, for the sampling logic and single turn DAQ: and the slower, 40 MHz for the bulk TBT data acquisition and transmission logic. The data is synchronised between the two clock domains before the channel sequencer. A 2.16 MHz signal synchronised to the DR revolution period, is generated from a counter running on the 357 MHz and is used as a turn counter, with the option to use an external source of 2.16 MHz from the machine. The turn counter allows for the acquisition of n turns in every m in order to increase the range of the time window across the damping cycle, but retain the flexibility to record batches of consecutive turns within the window.

Every 14-bit bunch sample is read-out from the FIFO as two 7-bit words and transmitted by the UART at a rate of 460.8 kbps, taking a minimum of ~ 4 second to return the entire contents of the FIFO. TBT acquisition is initiated by the user through the DAQ front-end, and controlled by the FIFO status flags, *full* and *empty*. Acquisition will begin on the arrival of an injection trigger if the trigger system is armed and enabled by the DAQ, and will proceed until the *FIFO full* flag is asserted. This will trigger the data transmission though the UART. When the FIFO is completely read-out *FIFO-empty* is asserted and the trigger system is re-armed.

INITIAL RESULTS

Initial results from the system are shown below. Figure 2 shows a time window of the first few thousand consecutive turns after injection for a single (x-difference) channel of single bunch beam. Beam injection occurs at turn number 6 with respect to the injection trigger. Injection transients can clearly be seen, with a period of 200 turns (tune of 0.005), which corresponds to the synchrotron frequency of 10.8 kHz [5,6]. These oscillations are initially damped but appear to be excited in bursts, and remain at a low level through most sets of data recorded.

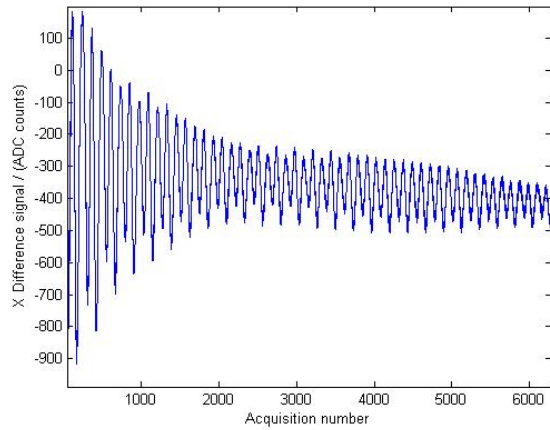


Figure 2: X difference signal for first few thousand turns of single bunch beam. Note injection occurs at turn number 6.

Figure 3 shows the corresponding data for multi-train beam, where due to the fill pattern in the DR, bunch 2 is the first injected, followed by 1 and then 3. This dataset shows a similar time window to Fig.1 but starting just before the injection of Bunch 3. Bunch 3 shows a similar pattern in term of synchrotron oscillations to that of Fig 2, however bunches 2 and 1 have been damping for 1 and 2 complete machine cycles respectively, and the magnitude of the oscillations is smaller although both bunches are clearly disturbed by the injection of Bunch 3.

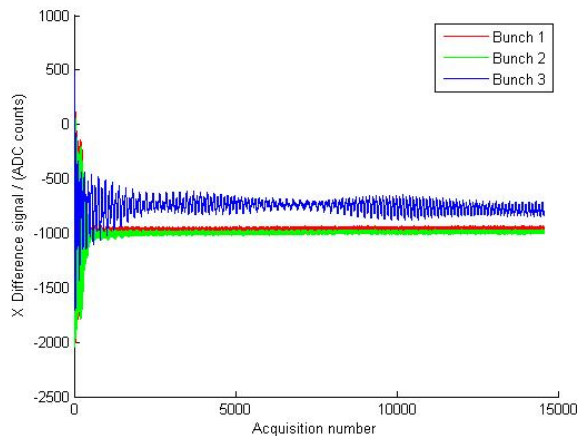


Figure 3: X difference signals for first few thousand turns of multi-train beam.

Figure 4 demonstrates the operation of the n -in- m mode, where 1 in every 32 turns is the granularity required to cover the entire damping cycle of a bunch in single train mode. As in Fig. 3 injection occurs at turn 6, and extraction at around turn 940,000. The mean transverse position in the DR appears to settle after about 100,000 turns.

Figure 5 shows the response of the system to a change in the mean orbit in the DR. In this case, an orbit bump was made across a region in close proximity to the BPM, using four corrector magnets. Five bump settings were made with a nominal range of +1 to -1 mm, and a linear

step size of 0.5 mm. At each setting 45,000 turns were recorded with a time window of consecutive turns near to, but not encompassing, the point of extraction. Note in this plot the data has been charge normalised and calibrated using the know calibration constant for the BPM processor.

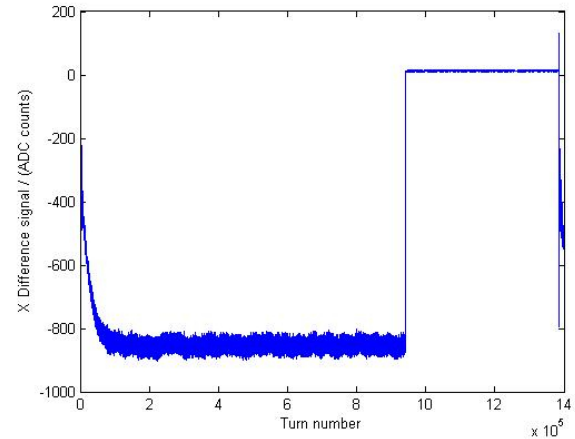


Figure 4: X difference signals for every 1 turn in 32 of single bunch beam. Note that injection occurs at turn 0 and extraction around turn number 940000. On the far right of the figure a subsequent injection can be seen, at a time of 0.65 s after the first, corresponding to the next machine cycle.

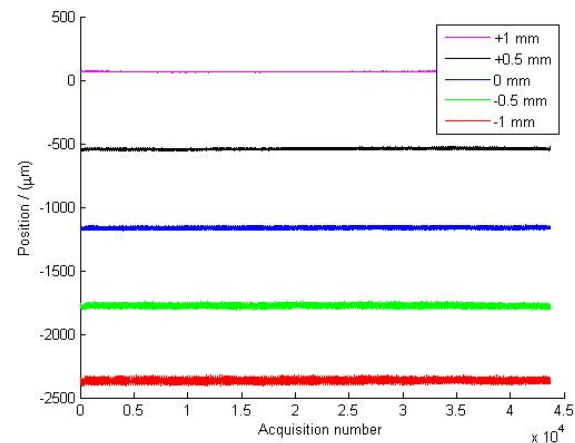


Figure 5: Vertical position for c. 45000 turns of single bunch beam, for five different vertical orbit bump settings.

REFERENCES

- [1] <http://www.linearcollider.org/cms/>
- [2] <http://clic-study.web.cern.ch/CLIC-Study/>
- [3] <http://www-atf.kek.jp/atf/>
- [4] R. Apsimon et al, Proceedings IPAC10, Kyoto, Japan, p. 2788.
- [5] M. Ross, B. Mellor, ATF Report, ATF-04-06,
- [6] M. Wendt et al, Proceedings of DIPAC09, Basel, Switzerland, p.89.